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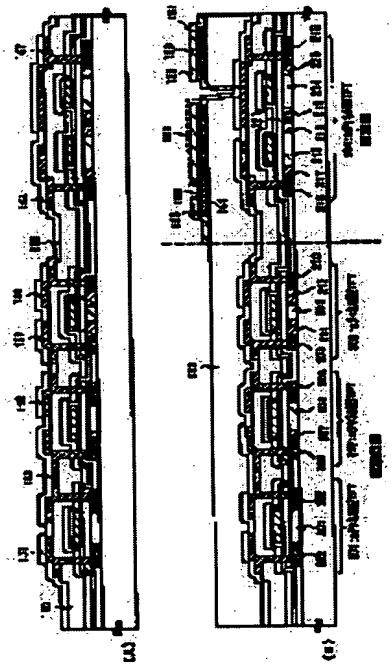
(54) ELECTRO-OPTICAL DEVICE AND PREPARATION THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To improve the effective aperture ratio by forming an offset region between channel and LDD regions, such that the LDD region of a drive TFT overlaps with a gate interconnection through a gate insulating film, and such that the LDD region of a pixel TFT does not overlap with the gate interconnection sandwiching the gate insulating film.

SOLUTION: A drive circuit is provided with a p channel TFT(thin-film transistor) 301, and an n channel TFT 302 and 303, while a pixel section is provided with a pixel TFT 304 formed of an n channel TFT. The TFT 302 is provided with an LDD region 207, which is located between a channel forming region 204 and a drain region 206, and which overlaps with a gate interconnection sandwiching a gate insulating film. Furthermore, the TFT 304 is provided with



regions 217 to 220 and an offset region 221, which do not overlap with the gate interconnection through via channel-forming regions 213 and 214, a source region 215, a drain region 216, and the gate insulating film.

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CLAIMS

[Claim(s)]
[Claim 1] The LDD field of the n channel mold TFT which forms said drive circuit in an electro-optic device including the pixel section and a drive circuit on the same substrate The LDD field of the pixel TFT which is formed so that a part or all may lap with gate wiring of this n channel mold TFT on both sides of gate dielectric film, and forms said pixel section The electro-optic device characterized by being formed so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film, and forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[Claim 2] The LDD field of the n channel mold TFT which forms said drive circuit in an electro-optic device including the pixel section and a drive circuit on the same substrate The LDD field of the pixel TFT which is formed so that a part or all may lap with gate wiring of this n channel mold TFT on both sides of gate dielectric film, and forms said pixel section It is formed so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film. The retention volume of said pixel section is an electro-optic device characterized by being formed with the oxide and the pixel electrode of a screen and this screen which were prepared on the organic resin film, and forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[Claim 3] The electro-optic device characterized by containing n mold impurity element by concentration higher than the LDD field of said pixel TFT in claim 1 or claim 2 in the LDD field of the n channel mold TFT which forms said drive circuit.
[Claim 4] The electro-optic device characterized by containing n mold impurity element by one 2 to 10 times the concentration of this compared with the LDD field of said pixel TFT in claim 1 or claim 2 in the LDD field of the n channel mold TFT which forms said drive circuit.
[Claim 5] The electro-optic device characterized by containing n mold impurity element in claim 1 or claim 2 by the density range of 2x1016 - 5x1019 atoms/cm3 in the LDD field of the n channel mold TFT which forms said drive circuit, and containing n mold impurity element in the LDD field of said pixel TFT by the density range of 1x1016 - 5x1018 atoms/cm3.
[Claim 6] In the electro-optic device which includes the pixel section and a drive circuit on the same substrate in said drive circuit The 1st n channel mold TFT formed so that all of LDD fields might lap with gate wiring on both sides of gate dielectric film, The LDD field of the pixel TFT which has the 2nd n channel mold TFT formed so that a part of LDD field might lap with gate wiring on both sides of gate dielectric film, and forms said pixel section The electro-optic device characterized by being arranged so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film, and forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[Claim 7] In the electro-optic device which includes the pixel section and a drive circuit on the same substrate in said drive circuit The 1st n channel mold TFT formed so that all of LDD fields might lap with gate wiring on both sides of gate dielectric film, The LDD field of the pixel TFT which has the 2nd n channel mold TFT formed so that a part of LDD field might lap with gate wiring on both sides of gate dielectric film, and forms said pixel section It is arranged so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film. The retention volume of said pixel section is an electro-

optic device characterized by being formed with the oxide and the pixel electrode of a screen and this screen which were prepared on the organic resin film, and forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[Claim 8] The electro-optic device characterized by containing n mold impurity element by concentration higher than the LDD field of said pixel TFT in said 1st n channel type TFT of LDD field, and/or said 2nd n channel type TFT of LDD field in claim 6 or claim 7.
[Claim 9] The electro-optic device characterized by containing n mold impurity element by one 2 to 10 times the concentration of this compared with the LDD field of said pixel TFT in claim 6 or claim 7 in said 1st n channel type TFT of LDD field, and/or said 2nd n channel type TFT of LDD field.
[Claim 10] the LDD field formed in said 1st n channel mold TFT in claim 6 or claim 7 -- this -- the LDD field which is formed between the drain field of the 1st n channel mold TFT, and a channel formation field, and is formed in said 2nd n channel mold TFT -- this -- the electro-optic device characterized by being formed across the channel formation field of the 2nd n channel mold TFT.
[Claim 11] The electro-optic device characterized by containing n mold impurity element by the density range of 2x1016 - 5x1019 atoms/cm3 in said 1st n channel type TFT of LDD field, and/or said 2nd n channel type TFT of LDD field, and containing n mold impurity element in the LDD field of said pixel TFT in claim 6 or claim 7 by the density range of 1x1016 - 5x1018 atoms/cm3.
[Claim 12] It is the electro-optic device characterized by consisting of semi-conductor film of the same presentation as the channel formation field where said offset field touched this offset field in any 1 of claim 1, claim 2, claim 6, or claims 7.
[Claim 13] The electro-optic device characterized by containing p mold impurity element in said offset field by the density range of 1x1015 - 1x1018 atoms/cm3 in any 1 of claim 1, claim 2, claim 6, or claims 7.
[Claim 14] It is the electro-optic device characterized by being the film with which said screen uses the aluminum film or aluminum as a principal component in claim 2 or claim 7.
[Claim 15] The electro-optic device characterized by said oxide being the aluminum-oxide film in claim 2 or claim 7.
[Claim 16] The electro-optic device characterized by having an EL element in said pixel section in any 1 of claim 1 thru/or claims 15.
[Claim 17] The electric appliance characterized by using an electro-optic device according to claim 1 to 16 as a display.
[Claim 18] In the production approach of the electro-optic device which includes the pixel section and a drive circuit on the same substrate The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 2x1016 - 5x1019 atoms/cm3 (A), The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 1x1020 - 1x1021 atoms/cm3 (B), The process which forms the field which contains p mold impurity element in the barrier layer of the p channel mold TFT which forms said drive circuit by the density range of 3x1020 - 3x1021 atoms/cm3 (C), The process which forms the field which contains n mold impurity element in the barrier layer of the pixel TFT which forms said pixel section by the density range of 1x1016 - 5x1018 atoms/cm3 (D), It is the production approach of the electro-optic device characterized by being carried out by ****(ing), and said process's (D's)'s using as a mask gate wiring covered by the insulator layer containing silicon, and adding n mold impurity element.
[Claim 19] In the production approach of the electro-optic device which includes the pixel section and a drive circuit on the same substrate The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 2x1016 - 5x1019 atoms/cm3 (A), The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 1x1020 - 1x1021 atoms/cm3 (B), The process which forms the field which contains p mold impurity element in the barrier layer of the p channel mold TFT which forms said drive circuit by the density range of 3x1020 - 3x1021 atoms/cm3 (C), The process which forms the field which contains

n mold impurity element in the barrier layer of the pixel TFT which forms said pixel section by the density range of 1x1016 - 5x1018 atoms/cm3 (D), The production approach of the electro-optic device characterized by forming the offset field which ****(ed) and touched n mold impurity range (c) and this n mold impurity range (c) according to said process (D).
[Claim 20] The thickness of the insulator layer which contains said silicon in claim 18 is the production approach of the electro-optic device characterized by being 25-100nm.
[Claim 21] It is the production approach of the electro-optic device characterized by being formed by using as a mask gate wiring covered by the insulator layer to which said offset field contains silicon in the barrier layer of said pixel TFT in claim 19, and adding n mold impurity element.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which has the circuit which consisted of thin film transistors (henceforth TFT) on the substrate which has an insulating front face, and its production approach. Especially this invention relates to the electric appliance (it is also called electronic equipment) carrying the liquid crystal display which prepared the pixel section (pixel circuit) and the drive circuit (control circuit) prepared around it on the same substrate, the electro-optic device (it is also called an electro-optic device) represented by EL (electroluminescence) display, and an electro-optic device.
[0002] In addition, in this application specification, a semiconductor device points out the equipment at large which functions by using a semi-conductor property, and the electric appliance carrying the above-mentioned electro-optic device and its electro-optic device is also contained in a semiconductor device.
[0003]
[Description of the Prior Art] Development of the semiconductor device which has the large area integrated circuit formed by TFT on the substrate which has an insulating front face is progressing. The active matrix liquid crystal indicating equipment, EL indicating equipment, and the contact type image sensor are known as the example of representation. Especially TFT (it is hereafter described as poly-Si TFT) that made the barrier layer the crystalline substance silicon film (typically polish recon film) can also form various functional circuits from electric field effect mobility being high.
[0004] For example, the drive circuit (called a circumference drive circuit) for controlling the pixel sections, such as the pixel section which performs image display for every functional block, and a shift register based on a CMOS circuit, a level shifter, a buffer, a sampling circuit, to an active matrix liquid crystal indicating equipment is formed on one substrate.
[0005] Since such a drive circuit does not necessarily have the same operating condition in each, the properties naturally required of TFT also differ not a little. It is the pixel TFT which functions as a switching device, and the configuration of having prepared auxiliary retention volume, and liquid crystal is made to impress and drive an electrical potential difference in the pixel section. Here, it is necessary to make liquid crystal drive by alternating current, and many methods called a frame reversal drive are adopted. Therefore, the property of TFT demanded needed to make sufficiently low the OFF state current value (drain current value to which TFT flows at the time of off actuation). Moreover, since high driver voltage was impressed, the buffer needed to raise pressure-proofing even to extent which does not break even if the high voltage is built. Moreover, in order to heighten current drive capacity, the ON state current value (drain current value to which TFT flows at the time of ON actuation) needed to be secured enough.
[0006] However, the OFF state current value of poly-Si TFT has the trouble of being easy to become high. Moreover, the degradation phenomenon of the fall of an ON state current value is observed by poly-Si TFT like the MOS transistor used by IC etc. A main cause is hot carrier impregnation and the hot carrier generated by the high electric field near the drain is considered to cause a degradation

phenomenon.
[0007] Low concentration drain (LDD:Lightly Doped Drain) structure is known as structure of TFT for reducing an OFF state current value. This structure prepares a low-concentration impurity range between a channel formation field, and the source field or drain field where an impurity is added by high concentration, and this low concentration impurity range is called the LDD field.
[0008] Moreover, the so-called GOLD (Gate-drain Overlapped LDD) structure is known as structure for preventing degradation of the ON state current value by hot carrier impregnation. Since this structure is arranged so that a LDD field may lap with gate wiring through gate dielectric film, it is effective in preventing the hot carrier impregnation near the drain and raising dependability. For example, although the GOLD structure by the sidewall formed with silicon is indicated in "Mutsuko Hatano, Hajime Akimoto and Takeshi Sakai, IEDM97 TECHNICAL DIGEST, p523-526, and 1997", it is checked that the extremely excellent dependability is acquired compared with TFT of other structures.
[0009] Moreover, TFT is arranged at each dozens to millions of pixel at the pixel section of an active matrix liquid crystal display, and the pixel electrode is prepared in the each of TFT. The counterelectrode is prepared in the opposite substrate side which sandwiched liquid crystal, and a kind of capacitor which used liquid crystal as the dielectric is formed. And liquid crystal is driven by controlling the electrical potential difference impressed to each pixel by the switching function of TFT, and controlling the charge to this capacitor, and it has become the structure which controls the amount of transmitted lights and displays an image.
[0010] However, this capacitor had become the cause by which the amount of transmitted lights changed and the contrast of image display was reduced, in order that that storage capacitance might decrease gradually according to the leakage current resulting from an OFF state current value etc. So, capacity wiring was prepared, the capacitor (retention volume) other than the capacitor which uses liquid crystal as a dielectric was formed in juxtaposition, and the capacity which the capacitor which uses liquid crystal as a dielectric loses was compensated with the former.
[0011]
[Problem(s) to be Solved by the Invention] However, the property demanded is not necessarily the same at TFT (henceforth Pixel TFT) of the pixel section, and TFT (henceforth Drive TFT) of drive circuits, such as a shift register and a buffer. For example, in Pixel TFT, although a big reverse bias (it will subtract if it is n channel mold TFT) electrical potential difference is impressed to gate wiring, a reverse bias electrical potential difference is impressed fundamentally, and TFT of a drive circuit does not operate. Moreover, as for the former working speed, as high a thing as the latter is not required.
[0012] Moreover, although the effectiveness that surely GOLD structure prevents degradation of an ON state current value was high, on the other hand, there was a problem to which an OFF state current value becomes large compared with the usual LDD structure. Therefore, especially for Pixel TFT, it was not able to be said to be desirable structure. Conversely, the weak thing was known by hot carrier impregnation although the effectiveness that the usual LDD structure holds down an OFF state current value was high.
[0013] Thus, in the electro-optic device which has two or more electrical circuits like an active matrix liquid crystal display, it was not necessarily desirable to have formed all TFT(s) with the same structure.

[0014] Furthermore, as shown in the conventional example, when the retention volume which used capacity wiring for the pixel section tended to be formed and it was going to secure sufficient capacity, the numerical aperture (area to an area of 1 pixel in which image display is possible comparatively) had to be sacrificed. Especially by small highly minute panel which is used for a projector mold display, since the pixel area per piece was also small, the decline in the numerical aperture by capacity wiring had become a problem.
[0015] This invention is a technique for solving such a technical problem, and it aims at raising the engine performance of operation and dependability of an electro-optic device by making suitable structure of TFT arranged at the drive circuit and the pixel section of an electro-optic device according to the function. Moreover, let it be a technical problem to offer the production approach for realizing

such an electro-optic device.
[0016] Moreover, in the electro-optic device which has the pixel section as other purposes, area of the retention volume prepared in a pixel is contraction-ized, and it aims at offering the structure for raising a numerical aperture. Moreover, the production approach of such the pixel section is offered.
[0017]
[Means for Solving the Problem] In order to solve the above-mentioned trouble the configuration of this invention The LDD field of the n channel mold TFT which forms said drive circuit in an electro-optic device including the pixel section and a drive circuit on the same substrate The LDD field of the pixel TFT which is formed so that a part or all may lap with gate wiring of this n channel mold TFT on both sides of gate dielectric film, and forms said pixel section It is characterized by being formed so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film, and forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[0018] In the above-mentioned configuration, it is desirable that n mold impurity element is contained by concentration higher than the LDD field of said pixel TFT in the LDD field of the n channel mold TFT which forms said drive circuit. Specifically, one 2 to 10 times the concentration of this is more desirable than the LDD field of said pixel TFT. In the LDD field of the n channel mold TFT which forms said drive circuit, n mold impurity element is still more specifically contained by the density range of 2x1016 - 5x1019 atoms/cm3, and n mold impurity element is contained in the LDD field of said pixel TFT by the density range of 1x1016 - 5x1018 atoms/cm3.
[0019] In the electro-optic device with which the configuration of other invention includes the pixel section and a drive circuit on the same substrate moreover, in said drive circuit The 1st n channel mold TFT formed so that all of LDD fields might lap with gate wiring on both sides of gate dielectric film, The LDD field of the pixel TFT which has the 2nd n channel mold TFT formed so that a part of LDD field might lap with gate wiring on both sides of gate dielectric film, and forms said pixel section It is arranged so that it may not lap with gate wiring of this pixel TFT on both sides of gate dielectric film, and it is characterized by forming the offset field between the channel formation field of said pixel TFT, and a LDD field.
[0020] In the above-mentioned configuration, n mold impurity element is contained by concentration (specifically two to 10 times) higher than the LDD field of said pixel TFT in said 1st n channel type TFT of LDD field, and/or said 2nd n channel type TFT of LDD field.
[0021] moreover, the LDD field formed in said 1st n channel mold TFT -- this -- the LDD field which is formed between the drain field of the 1st n channel mold TFT, and a channel formation field, and is formed in said 2nd n channel mold TFT -- this -- it is desirable to be formed across the channel formation field of the 2nd n channel mold TFT.
[0022] Moreover, the configuration about the production process for realizing the configuration of the invention in this application In the production approach of the electro-optic device which includes the pixel section and a drive circuit on the same substrate The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 2x1016 - 5x1019 atoms/cm3 (A), The process which forms the field which contains n mold impurity element in the barrier layer of the n channel mold TFT which forms said drive circuit by the density range of 1x1020 - 1x1021 atoms/cm3 (B), The process which forms the field which contains p mold impurity element in the barrier layer of the p channel mold TFT which forms said drive circuit by the density range of 3x1020 - 3x1021 atoms/cm3 (C), The process which forms the field which contains n mold impurity element in the barrier layer of the pixel TFT which forms said pixel section by the density range of 1x1016 - 5x1018 atoms/cm3 (D), It is characterized by being carried out by ****(ing), and said process's (D's)'s using as a mask gate wiring covered by the insulator layer containing silicon, and adding n mold impurity element.
[0023] In addition, in this configuration, the sequence of each process of (A) - (D) may be changed suitably. The fundamental function of TFT finally formed as any sequence does not change, and does not spoil the effectiveness of this invention.
[0024]

[Embodiment of the Invention] Suppose that detailed explanation is given about the gestalt of operation of this invention as it is also at the example shown below.
[0025] The example of [example 1] this invention is explained using drawing 1 - drawing 4 . Here, how to produce the drive circuit for controlling the pixel section and its pixel section on the same substrate to coincidence is explained. However, in order to simplify explanation, suppose that the CMOS circuit which are basic circuits, such as a shift register and a buffer, and the n channel mold TFT which forms a sampling circuit are illustrated in a drive circuit.
[0026] In drawing 1 (A), it is desirable to use a quartz substrate and a silicon substrate for a substrate 101. A quartz substrate is used in this example. In addition, it is good also considering the thing in which the insulator layer was formed on the front face of a metal substrate or a stainless steel substrate, as a substrate. Since the thermal resistance which can bear the temperature of 800 degrees C or more is required in the case of this example, as long as it is the substrate which fills it, what kind of substrate may be used.
[0027] And the semi-conductor film 102 including amorphous structure with a thickness of 20-100nm (preferably 40-80nm) is formed in the front face in which TFT of a substrate 101 is formed by the method of reduced pressure heat CVD, the plasma-CVD method, or the spatter. In addition, although the amorphous silicon film of 60nm thickness is formed in this example, since a thermal oxidation process is behind, this thickness does not necessarily turn into thickness of the final barrier layer of TFT.
[0028] Moreover, as semi-conductor film including amorphous structure, there are amorphous semiconductor film and microcrystal semi-conductor film, and the compound semiconductor film which includes the amorphous structure of the amorphous silicon germanium film etc. further is also contained. Furthermore, it is also effective to form continuously without carrying out atmospheric-air release of the substrate film and the amorphous silicon film on a substrate. By doing so, contamination on the front face of a substrate can become able [not affect the amorphous silicon film] to make it, and the property variation of TFT produced can be reduced.
[0029] Next, on the amorphous silicon film 102, the mask film 103 which becomes by the insulator layer containing silicon (silicon) is formed, and Openings 104a and 104b are formed by patterning. This opening serves as an addition field for adding the catalyst element which promotes crystallization in the case of the following crystallization process (promotion). (Drawing 1 (A))
[0030] In addition, as an insulator layer containing silicon, the silicon oxide film, a silicon nitride film, and the nitriding silicon oxide film can be used. The nitriding silicon oxide film is an insulator layer which contains silicon, nitrogen, and oxygen in a predetermined amount, and is an insulator layer expressed with SiOxNy. The nitriding silicon oxide film can produce SiH4, N2O, and NH3 as material gas, and is good for the nitrogen concentration to contain to consider as less than [more than 25atomic% 50atomic%].
[0031] Moreover, the marker pattern used as the criteria of a next patterning process is formed at the same time it performs patterning of this mask film 103. Although the amorphous silicon film 102 is also slightly etched in case the mask film 103 is etched, this level difference can use as a marker pattern behind at the time of mask alignment.
[0032] Next, according to the technique indicated by JP,10-247735,A (it corresponds to the U.S. application number 09 / 041), the semi-conductor film including the crystal structure is formed. [034 and 041] A technique given [this] in an official report is a crystallization means using the catalyst element (a kind or two or more sorts of elements chosen from nickel, cobalt, germanium, tin, lead, palladium, iron, and copper) which promotes crystallization on the occasion of crystallization of the semi-conductor film including amorphous structure.
[0033] It heat-treats in the condition of having made the catalyst element specifically holding on the front face of the semi-conductor film including amorphous structure, and the semi-conductor film including amorphous structure is changed to the semi-conductor film including the crystal structure. In addition, as a crystallization means, the technique indicated by the example 1 of JP,7-130652,A may be used. Moreover, although the so-called single crystal semiconductor film and the polycrystal semi-conductor film are contained in the semi-conductor film including crystalline substance structure, the

semi-conductor film including the crystal structure formed in this official report has the grain boundary.
[0034] In addition, although the spin coat method is used in this official report in case the layer containing a catalyst element is formed on the mask film, it is very good in a means to form membranes using gaseous-phase methods [thin film / containing a catalyst element], such as a spatter and vacuum deposition.
[0035] Moreover, although the amorphous silicon film is based also on the amount of content hydrogen, it is desirable to make it crystallize, since heat-treatment of about 1 hour is preferably performed at 400-550 degrees C and hydrogen is fully desorbed. In that case, it is desirable to make the amount of content hydrogen into less than [5atom%].
[0036] After a crystallization process performs the heat treatment process of about 1 hour at 400-500 degrees C first and desorbs hydrogen out of the film, it performs heat treatment of 6 - 16 hours (preferably 8 - 14 hours) at 500-650 degrees C (preferably 550-600 degrees C).
[0037] At this example, heat treatment of 14 hours is performed at 570 degrees C, using nickel as a catalyst element. Consequently, crystallization advances with the openings 104a and 104b as the starting point in the direction (direction shown by the arrow head) parallel to an outline substrate, and the semi-conductor film (this example crystalline substance silicon film) 105a-105d including the crystal structure to which the macroscopic crystal growth direction was equal is formed. [(Drawing 1 (B))
0038] Next, the gettering process which removes the nickel used at the process of crystallization from the crystalline substance silicon film is performed. In this example, the process which adds the element (this example Lynn) which belongs to 15 groups of a periodic table by using as a mask the mask film 103 in which the point was formed as it is is performed, and the Lynn addition fields (henceforth a gettering field) 106a and 106b which include Lynn in the crystalline substance silicon film exposed by Openings 104a and 104b by the concentration of 1x1019 - 1x1020 atoms/cm3 are formed. (Drawing 1 (C))
[0039] Next, 450-650 degrees C (preferably 500-550 degrees C) and the heat treatment process of 4 - 24 hours (preferably 6 - 12 hours) are performed in nitrogen-gas-atmosphere mind. The nickel in the crystalline substance silicon film moves in the direction of an arrow head according to this heat treatment process, and it is captured to the gettering fields 106a and 106b according to a gettering operation of Lynn. That is, since nickel is removed out of the crystalline substance silicon film, the nickel concentration contained in the crystalline substance silicon film 107a-107d after gettering can be preferably reduced even to 1x1016 atms/cm3 three or less 1x1017 atms/cm.
[0040] Next, the mask film 103 is removed and a protective coat 108 is formed a sake [at the time of next impurity addition] on crystalline substance silicon film 107a-107d. A protective coat 108 is good to use the nitriding silicon oxide film or the silicon oxide film with a thickness of 100-200nm (preferably 130-170nm). This protective coat 108 has the semantics for enabling delicate concentration control, in order not to put the crystalline substance silicon film to the direct plasma at the time of impurity addition.
[0041] And the resist mask 109 is formed on it and the impurity element (henceforth p mold impurity element) which gives p mold through a protective coat 108 is added. Boron or a gallium can be used for the element and type target which belong to 13 groups of the periodic table typically as a p mold impurity element. This process (it is called a channel dope process) is a process for controlling the threshold electrical potential difference of TFT. In addition, boron is added by the ion doping method which carried out plasma excitation without carrying out mass separation of the diboron hexahydride (B-2 H6) here. Of course, the ion implantation method for performing mass separation may be used.
[0042] The impurity ranges 110a and 110b which contain p mold impurity element (this example boron) according to this process by the concentration of 1x1015 - 1x1018 atoms/cm3 (typically 5x1016 - 5x1017 atoms/cm3) are formed. In addition, in this specification, the impurity range (however, field where Lynn is not included) containing p mold impurity element is defined as p mold impurity range (b) by the above-mentioned density range. (Drawing 1 (D))
[0043] Next, the resist mask 109 is removed, patterning of the crystalline substance silicon film is carried out, and the island-like semi-conductor layers (henceforth a barrier layer) 111-114 are formed. In

addition, barrier layers 111-114 are formed very much by the crystalline good crystalline substance silicon film by adding nickel alternatively and crystallizing. Specifically, it has cylindrical or the crystal structure with which the column-like crystal had specific directivity and was located in a line. Moreover, the concentration of the catalyst element which is removing or reducing nickel according to a gettering operation of Lynn after crystallization, and remains in a barrier layer 111-14 is 1x1016 atms/cm3 preferably three or less 1x1017 atms/cm. (Drawing 1 (E))

[0044] Moreover, the barrier layer 111 of the p channel mold TFT is a field which does not contain the impurity element added intentionally, and the barrier layers 112-114 of the n channel mold TFT serve as p mold impurity range (b). In this specification, it is defined as the barrier layers 111-114 of this condition being genuineness genuineness or substantially altogether. That is, the field where the impurity element is intentionally added by extent which does not cause trouble to actuation of TFT may consider a genuineness field substantially.

[0045] Next, the insulator layer which contains the silicon of 10-100nm thickness by the plasma-CVD method or the spatter is formed. In this example, the nitriding silicon oxide film of 30nm thickness is formed. The insulator layer containing other silicon may be used for the insulator layer containing this silicon in a monolayer or a laminating.

[0046] Next, the heat treatment process of 15 minutes - 8 hours (preferably 30 minutes - 2 hours) is performed under an oxidizing atmosphere at the temperature of 800-1150 degrees C (preferably 900-1000 degrees C) (thermal oxidation process). In this example, 950-degree-C heat treatment process for 80 minutes is performed in the ambient atmosphere which added the hydrogen chloride of 3 volume % in the oxygen ambient atmosphere. In addition, the boron added at the process of drawing 1 (D) is activated between this thermal oxidation process. (Drawing 2 (A))

[0047] In addition, as an oxidizing atmosphere, although a dry oxygen ambient atmosphere or a wet oxygen ambient atmosphere is sufficient, the dry oxygen ambient atmosphere is suitable for reduction of the crystal defect in a semi-conductor layer. Moreover, although considered as the ambient atmosphere which included the halogen in the oxygen ambient atmosphere in this example, you may carry out in an oxygen ambient atmosphere 100%.

[0048] Also in the interface of the insulator layer containing silicon, and the barrier layers 111-114 under it, oxidation reaction advances between this thermal oxidation process. In the invention in this application, it adjusts so that the thickness of the gate dielectric film 115 finally formed in consideration of it may be set to 50-200nm (preferably 100-150nm). At the thermal oxidation process of this example, 25nm of the barrier layer of 60nm thickness oxidizes, and the thickness of barrier layers 111-114 is set to 45nm. Moreover, since the thermal oxidation film of 50nm thickness is added to the insulator layer containing the silicon of 30nm thickness, the thickness of final gate dielectric film 115 is set to 110nm.

[0049] Next, the resist masks 116-119 are newly formed. And the impurity ranges 120-122 which add the impurity element (henceforth n mold impurity element) which gives n mold, and present n mold are formed. In addition, Lynn or arsenic can be used for the element and type target which belong to 15 groups of a periodic table typically as an n mold impurity element. (Drawing 2 (B))

[0050] These impurity ranges 120-122 are impurity ranges for making it function as a LDD field in the n channel mold TFT of a CMOS circuit and a sampling circuit later. In addition, n mold impurity element is contained in the impurity range formed here by the concentration of 2x1016 - 5x1019 atoms/cm3 (typically 5x1017 - 5x1018 atoms/cm3). In this specification, the impurity range containing n mold impurity element is defined as n mold impurity range (b) by the above-mentioned density range.

[0051] In addition, Lynn is added by the concentration of 1x1018 atoms/cm3 by the ion doping method which carried out plasma excitation without carrying out mass separation of the phosphoretted hydrogen (PH3) here. Of course, the ion implantation method for performing mass separation may be used. At this process, Lynn is added on the crystalline substance silicon film through the gate film 115.

[0052] Next, Lynn which heat-treated in the 600-1000 degrees C (preferably 700-800 degrees C) inert atmosphere, and was added at the process of drawing 2 (B) is activated. In this example, 800-degree-C heat treatment of 1 hour is performed in nitrogen-gas-atmosphere mind. (Drawing 2 (C))

[0053] At this time, it is possible to restore the interface of the barrier layer and barrier layer which were

damaged in coincidence at the time of addition of Lynn, and gate dielectric film. Although this activation process has desirable furnace annealing which used the electric heat furnace, optical annealing, such as lamp annealing and laser annealing, may be used together.
[0054] it exists in the boundary section of n mold (impurity range b) 120-122, i.e., the perimeter of n mold impurity range (b), according to this process -- a joint with a genuineness field (of course, p mold impurity range (b) is included) becomes clear genuineness or substantially. This means that a LDD field and a channel formation field can form a very good joint, when TFT is completed behind.
[0055] Next, the electric conduction film used as gate wiring is formed. In addition, although gate wiring may be formed by the electric conduction film of a monolayer, it is desirable to consider as cascade screens, such as a bilayer and three layers, if needed. In this example, the cascade screen which becomes by the 1st electric conduction film 123 and the 2nd electric conduction film 124 is formed. (Drawing 2 (D))
[0056] Here as the 1st electric conduction film 123 and the 2nd electric conduction film 124 A tantalum (Ta), titanium (Ti), molybdenum (Mo), a tungsten (W), the electric conduction film (typical -- the tantalum nitride film --) which uses as a principal component chromium (Cr), the element chosen from silicon (Si), or said element The nitriding tungsten film, the titanium nitride film, or the alloy film (typically the Mo-W alloy film, Mo-Ta alloy film, tungsten silicide film, etc.) that combined said element can be used.
[0057] In addition, the 1st electric conduction film 123 is set to 10-50nm (preferably 20-30nm), and should just set the 2nd electric conduction film 124 to 200-400nm (preferably 250-350nm). In this example, the nitriding tungsten (WN) film of 50nm thickness is used as the 1st electric conduction film 123, and the tungsten film of 350nm thickness is used as the 2nd electric conduction film 124. In addition, although not illustrated, it is effective to form the silicon film on the 1st electric conduction film 123 or in the bottom by the thickness of about 2-20nm. Antioxidizing can be planned with improvement in the adhesion of the electric conduction film formed on it by this.
[0058] Moreover, it is also effective to use the tantalum film as the tantalum nitride film and the 2nd electric conduction film as the 1st electric conduction film 123.
[0059] Next, the 1st electric conduction film 123 and the 2nd electric conduction film 124 are etched by package, and the gate wiring 125-128 of 400nm thickness is formed. At this time, the gate wiring 126 and 127 of the n channel mold TFT of a drive circuit is formed so that it may lap on both sides of the part and gate dielectric film 115 of n mold (impurity range b) 120-122. This overlapping part serves as a Lov field behind. In addition, although the gate wiring 128a and 128b is visible to two, it is formed from one pattern connected continuously in practice in the cross section. (Drawing 2 (E))
[0060] Next, the resist mask 129 is formed and the impurity ranges 130 and 131 which add p mold impurity element (this example boron), and contain boron in high concentration are formed. At this example, boron is added by 3x1020 - 3x1021 atoms/cm3 (typically 5x1020 - 1x1021 atoms/cm3) concentration by the ion doping method (of course, the ion implantation method may be used) for having used diboron hexahydride (B-2 H6). In addition, in this specification, the impurity range containing p mold impurity element is defined as p mold impurity range (a) by the above-mentioned density range. (Drawing 3 (A))
[0061] Next, the resist mask 129 is removed and the resist masks 132-134 are formed for the field used as gate wiring and the p channel mold TFT in a wrap form. And the impurity ranges 135-141 which add n mold impurity element (this example Lynn), and include Lynn in high concentration are formed. Here, it carries out by the ion doping method (of course, the ion implantation method may be used) for having used phosphoretted hydrogen (PH3), and concentration of Lynn of this field is made into 1x1020 - 1x1021 atoms/cm3 (typically 2x1020 - 5x1021 atoms/cm3). (Drawing 3 (B))
[0062] In addition, in this specification, the impurity range containing n mold impurity element is defined as n mold impurity range (a) by the above-mentioned density range. Moreover, although Lynn or boron already added at the last process is contained in the field in which impurity ranges 135-141 were formed, since Lynn will be added by concentration high enough, it is not necessary to consider the effect of Lynn added at the last process, or boron. Therefore, in this specification, impurity ranges 135-

141 may be put in another way as n mold impurity range (a).
[0063] Next, the resist masks 132-134 are removed and the cap film 142 which becomes by the insulator layer containing silicon is formed. thickness -- 25-100nm (preferably 30-50nm) -- then, it is good. Suppose that the silicon nitride film of 25nm thickness is used in this example. Although the cap film 142 functions also as a protective coat which prevents oxidation of gate wiring at a next activation process, since stress will become strong and faults, such as film peeling, will occur if it forms too much thickly, it is desirable to be preferably referred to as 100nm or less.
[0064] Next, n mold impurity element (this example Lynn) is added in self align by using gate wiring 125-128 as a mask. In the formed impurity ranges 143-146, in this way, the concentration of 1 / 2 - 1/10 (typically 1 / 3 - 1/4) of said n mold impurity range (b) (-- however, 5 to 10 times as high concentration as the boron concentration added at the above-mentioned channel dope process -- typical -- 1x1016 - 5x1018 atoms/cm3 -- typical -- 3x1017 - 3x1018 atoms/cm3 --) -- it adjusts so that Lynn may be added. In addition, in this specification, the impurity range (however, p mold impurity range (a) is removed) containing n mold impurity element is defined as n mold impurity range (c) by the above-mentioned density range. (Drawing 3 (C))
[0065] Although Lynn will be added through the insulator layer (cascade screen of the cap film 142 and gate dielectric film 115) of 105nm thickness at this process, the cap film formed in the side attachment wall of the gate wiring 134a and 134b also functions as a mask. That is, the offset field of the die length equivalent to the thickness of the cap film 142 will be formed. in addition, although it is formed in a channel formation field in contact with an offset field and becomes by the semi-conductor film of the same presentation as a channel formation field, since gate voltage is not impressed, an inversion layer (channel field) is not formed -- high -- a field [****] is pointed out. It can be said that it is important to suppress the lap of a LDD field and gate wiring as much as possible in order to lower an OFF state current value, and it is effective to prepare an offset field in such semantics.
[0066] In addition, like this example, when p mold impurity element is included by the concentration of 1x1015 - 1x1018 atoms/cm3 also to the channel formation field, naturally p mold impurity element is contained by this concentration also to an offset field.
[0067] Although the die length of this offset field is decided by the surroundings lump phenomenon at the time of adding the thickness and the impurity element of the cap film which are actually formed in the side attachment wall of gate wiring (phenomenon in which an impurity is added so that it may be hidden under a mask) If it carries out from a viewpoint of suppressing the lap of a LDD field and gate wiring, in case n mold impurity range (c) will be formed like the invention in this application, it is very effective to form the cap film beforehand.
[0068] In addition, although Lynn is added by all impurity ranges by the concentration of 1x1016 - 5x1018 atoms/cm3 except for the part hidden with gate wiring in this process, since it is very low concentration, the function of each impurity range is not affected. Moreover, although the boron of the concentration of 1x1015 - 1x1018 atoms/cm3 is already added by n mold (impurity range b) 143-146 at the channel dope process, since Lynn is added with boron 5 to 10 times the concentration of being contained at this process in p mold impurity range (b), you may think that boron does not affect the function of n mold impurity range (b) in this case, either.
[0069] however -- strict -- n mold impurity range (b) -- to the Lynn concentration of the part which lapped with gate wiring among 147 and 148 continuing being 2x1016 - 5x1019 atoms/cm3, Lynn of the concentration of 1x1016 - 5x1018 atoms/cm3 has joined it, and the part which does not lap with gate wiring will include Lynn by concentration high a little.
[0070] Next, the 1st interlayer insulation film 149 is formed. What is necessary is just to form as the 1st interlayer insulation film 149 by the insulator layer containing silicon, and the cascade screen which specifically combined a silicon nitride film, the silicon oxide film, the nitriding silicon oxide film, or them. Moreover, thickness is just 100-400nm. In this example, SiH4, N2O, and NH3 are made into material gas by the plasma-CVD method, and the nitriding silicon oxide film (however, nitrogen concentration 25 - 50atomic%) of 200nm thickness is used.
[0071] Then, in order to activate n mold or p mold impurity element added by each concentration, the

heat treatment process was performed. This process can use together the furnace annealing method, the laser annealing method, the lamp annealing method, or them, and can perform them. What is necessary is just to perform 500-800 degrees C at 550-600 degrees C preferably into an inert atmosphere, when carrying out by the furnace annealing method. In this example, 600 degrees C and heat treatment of 4 hours are performed, and an impurity element is activated. (Drawing 3 (D))

[0072] In addition, in this example, where the laminating of a silicon nitride film 142 and the nitriding silicon oxide film 149 is carried out, gate wiring is covered, and the activation process is performed in the condition. Although the tungsten is used as a wiring material in this example, it is known that the tungsten film is very weak to oxidation. That is, if a pinhole exists in a protective coat even if it covers and oxidizes by the protective coat, it will oxidize immediately. However, in this example, since the laminating of the nitriding silicon oxide film is carried out to the silicon nitride film, using the very effective silicon nitride film as antioxidizing film, it is possible to perform an activation process at high temperature, without caring about the problem of the pinhole of a silicon nitride film.

[0073] Next, after an activation process, in the ambient atmosphere containing 3 - 100% of hydrogen, heat treatment of 1 - 4 hours is performed at 300-450 degrees C, and a barrier layer is hydrogenated. This process is a process which carries out termination of the dangling bond of a semi-conductor layer by the hydrogen excited thermally. As other means of hydrogenation, plasma hydrogenation (the hydrogen excited by the plasma is used) may be performed.

[0074] If an activation process is finished, the 2nd interlayer insulation film 150 of 500nm - 1.5 micrometer thickness will be formed on the 1st interlayer insulation film 149. In this example, the silicon oxide film of 800nm thickness is formed by the plasma-CVD method as the 2nd interlayer insulation film 150. In this way, the interlayer insulation film of 1-micrometer thickness which becomes by the cascade screen of the 1st interlayer insulation film (nitriding silicon oxide film) 149 and the 2nd interlayer insulation film (silicon oxide film) 150 is formed.

[0075] In addition, if thermal resistance allows at a next process, it is also possible as the 2nd interlayer insulation film 150 to use organic resin film, such as polyimide, an acrylic, a polyamide, polyimidoamide, and BCB (benz-cyclo-butene).

[0076] Then, the contact hole which arrives at each source field or drain field of TFT is formed, and source wiring 151-154 and the drain wiring 155-157 are formed. In addition, in order to form a CMOS circuit, the drain wiring 155 is communalized between the p channel mold TFT and the n channel mold TFT. Moreover, although not illustrated, in this example, it considers as the cascade screen of the three-tiered structure which formed continuously 500nm of aluminum film which includes [Ti film] this wiring for 200nm and Ti, and 100nm of Ti film by the spatter. In addition, the laminating of copper wiring and the titanium nitride wiring may be carried out as source wiring or drain wiring. (Drawing 4 (A))

[0077] Next, it forms as passivation film 158 by the thickness of 50-500nm (typically 200-300nm) with a silicon nitride film, the silicon oxide film, or the nitriding silicon oxide film. At this time, by this example, plasma treatment is performed using the gas which contains H2 and NH3 grade hydrogen in advance of membranous formation, and it heat-treats after membrane formation. The hydrogen excited by this pretreatment is supplied into the 1st and 2nd interlayer insulation film. By heat-treating in this condition, since the hydrogen added in the 1st and 2nd interlayer insulation film is spread in a lower layer side while improving the membraneous quality of the passivation film 158, a barrier layer can be hydrogenated effectively.

[0078] Moreover, after forming the passivation film 158, a hydrogenation process may be performed further. For example, the same effectiveness is acquired, even if it is good to perform heat treatment of 1 - 12 hours at 300-450 degrees C or uses the plasma hydrogenating method in the ambient atmosphere containing 3 - 100% of hydrogen. In addition, opening (not shown) may be formed in the passivation film 158 in the location which forms the contact hole for connecting drain wiring with a pixel electrode after a hydrogenation process.

[0079] Then, the 3rd interlayer insulation film 159 which consists of organic resin is formed in the thickness of about 1 micrometer. As organic resin, polyimide, an acrylic, a polyamide, polyimidoamide,

BCB (benz-cyclo-butene), etc. can be used. The point for the membrane formation approach that the advantage of using the organic resin film is simple, the point that parasitic capacitance can be reduced since specific inductive capacity is low, the point of excelling in surface smoothness, etc. are got. In addition, the organic resin film except having mentioned above, an organic system SiO compound, etc. can also be used. Here, it calcinates and forms at 300 degrees C after applying to a substrate using the polyimide of the type which carries out thermal polymerization.

[0080] Next, in the field used as the pixel section, a screen 160 is formed on the 3rd interlayer insulation film 159. In addition, in this specification, **** called a screen is used for the purpose of interrupting light and an electromagnetic wave. A screen 160 forms in the thickness of 100-300nm the film which becomes by the element chosen from aluminum (aluminum), titanium (Ti), and a tantalum (Ta), or one of elements by the film used as a principal component. In this example, the aluminum film which made 1wt% titanium contain is formed in the thickness of 125nm.

[0081] In addition, if 5-50nm of insulator layers, such as silicon oxide film, is formed on the 3rd interlayer insulation film 159, the adhesion of the screen formed on this can be raised. Moreover, if plasma treatment which used CF4 gas for the front face of the 3rd interlayer insulation film 159 formed by organic resin is performed, the adhesion of the screen formed on the film by surface treatment can be raised.

[0082] Moreover, it is also possible to form not only a screen but other connection wiring using the aluminum film which made this titanium contain. For example, connection wiring which connects between circuits in a drive circuit can be formed. However, before forming the ingredient which forms a screen or connection wiring in that case, it is necessary to form a contact hole in the 3rd interlayer insulation film beforehand.

[0083] Next, the oxide 161 with a thickness of 20-100nm (preferably 30-50nm) is formed in the front face of a screen 160 by the anode oxidation method or the plasma oxidation method (this example anode oxidation method). In this example, since the film which uses aluminum as a principal component as a screen 160 was used, the aluminum-oxide film (alumina film) is formed as an anodic oxidation object 161.

[0084] On the occasion of this anodizing, a tartaric-acid ethylene glycol solution with alkali ion concentration small first fully is produced. This is the solution which mixed 15% of ammonium tartrate water solution, and ethylene glycol by 2:8, it adds aqueous ammonia to this, and it adjusts it so that pH may be set to 7**0.5. And the platinum electrode used as cathode is prepared into this solution, the substrate with which the screen 160 is formed is dipped in a solution, and the direct current of regularity (several mA - dozens of mA) is passed by making a screen 160 into an anode plate.

[0085] Although the electrical potential difference between the cathode in a solution and an anode plate changes with time amount according to growth of an anodic oxidation object, an electrical potential difference is raised at the pressure-up rate of 100 V/min with constant current, and anodizing is terminated in the place which amounted to attainment electrical-potential-difference 45V. Thus, the anodic oxidation object 161 with a thickness of about 50nm can be formed in the front face of a screen 160. Moreover, as a result, the thickness of a screen 160 is set to 90nm. In addition, it does not pass over the numeric value concerning the anode oxidation method shown here to an example, but, naturally an optimum value may change with the magnitude of the component to produce etc.

[0086] Moreover, although considered as the configuration which prepares an insulator layer only in a screen front face using an anode oxidation method here, an insulator layer may be formed by gaseous-phase methods, such as a plasma-CVD method, a heat CVD method, or a spatter. It is desirable that thickness sets to 20-100nm (preferably 30-50nm) also in that case. Moreover, the silicon oxide film, a silicon nitride film, the nitriding silicon oxide film, the DLC (Diamond like carbon) film, the tantalum oxide film, or the organic resin film may be used. Furthermore, the cascade screen which combined these may be used.

[0087] Next, the contact hole which reaches the drain wiring 157 is formed in the 3rd interlayer insulation film 159 and the passivation film 158, and the pixel electrode 162 is formed. In addition, the pixel electrode 163 is a pixel electrode of adjoining another pixel. A metal membrane should just be

used for the pixel electrodes 162 and 163 when making it into the liquid crystal display of a reflective mold using the transparence electric conduction film, in making it into a transparency mold liquid crystal display. Here, in order to consider as the liquid crystal display of a transparency mold, the compound (referred to as ITO) film of indium oxide and the tin oxide is formed in the thickness of 110nm by the spatter.

[0088] Moreover, at this time, the pixel electrode 162 and a screen 160 lap through the anodization object 161, and form retention volume (capacitance storage) 164. In addition, it is desirable in this case floating (condition isolated electrically), fixed potential, and to set a screen 160 as common potential (middle potential of the picture signal sent as data) preferably.

[0089] In this way, on the same substrate, the active-matrix substrate with a drive circuit and the pixel section was completed. In addition, in drawing 4 (B), the p channel mold TFT301 and the n channel mold 302 and TFT 303 are formed in a drive circuit, and the pixel TFT304 which becomes with the n channel mold TFT is formed in the pixel section.

[0090] The channel formation field 201, the source field 202, and the drain field 203 are formed in the p channel mold TFT301 of a drive circuit in p mold impurity range (a), respectively. However, Lynn is strictly included by the concentration of 1x1016 - 5x1018 atoms/cm3 to source 202 field and the drain field 203.

[0091] Moreover, the LDD field which lapped with the n channel mold TFT302 with gate wiring on both sides of gate dielectric film between the channel formation field 204, the source field 205, the drain field 206, and a channel formation field and a drain field (in this specification, such a field is called Lov field.) In addition, ov was attached in the sense of overlap. 207 is formed. At this time, the Lov field 207 is formed so that it may all lap with gate wiring by the concentration of 2x1016 - 5x1019 atoms/cm3, including Lynn.

[0092] Moreover, although the Lov field is arranged only in one side of the channel formation field 204 in drawing 4 (B) in order to reduce a resistance component as much as possible (only in case of drain field side), you may arrange on both sides across the channel formation field 204.

[0093] Moreover, as the channel formation field 208, the source field 209, the drain field 210, and a channel formation field are inserted into the n channel mold TFT303, the LDD fields 211 and 212 are formed in it. That is, a LDD field is formed between a source field and a channel formation field and between a drain field and a channel formation field.

[0094] In addition, the field which does not lap with the field (Lov field) which lapped with gate wiring through gate dielectric film, and gate wiring since it has been arranged so that a part of LDD fields 211 and 212 may lap with gate wiring with this structure (in this specification, such a field is called Loff field.) In addition, off was attached in the sense of offset. It realizes.

[0095] The sectional view shown in drawing 6 here is an enlarged drawing showing the condition of having produced the n channel mold TFT303 shown in drawing 4 (B) to the process of drawing 3 (C). As shown here, the LDD field 211 is further distinguishable to Lov field 211a and Loff field 211b. Moreover, although Lynn is included in the above-mentioned Lov field 211a by the concentration of 2x1016 - 5x1019 atoms/cm3, as for Loff field 211b, Lynn is included by the one to 2 twice (typically 1.2 to 1.5 times) as many concentration as this.

[0096] moreover -- a pixel -- TFT -- 304 -- **** -- a channel -- formation -- a field -- 213 -- 214 -- the source -- a field -- 215 -- a drain -- a field -- 216 -- Loff -- a field -- 217 - 220 -- Loff -- a field -- 218 -- 219 -- having touched -- n -- a mold -- an impurity range -- (-- a --) -- 221 -- forming -- having . At this time, the source field 215 and the drain field 216 are formed in n mold impurity range (a), respectively, and the Loff fields 217-220 are formed in n mold impurity range (c).

[0097] In this example, the structure of TFT which forms each circuit according to the circuit specification which the pixel section and a drive circuit require can be optimized, and the engine performance of operation and dependability of a semiconductor device can be raised. Specifically, the n channel mold TFT can realize TFT structure which thought high-speed operation or the cure against a hot carrier as important on the same substrate, and TFT structure which thought low OFF state current actuation as important by changing arrangement of a LDD field according to a circuit specification, and

using a Lov field or a Loff field properly.
[0098] For example, in the case of the active matrix liquid crystal indicating equipment, the n channel mold TFT302 fits drive circuits, such as a shift register which thinks high-speed operation as important, a subharmonics circuit, a signal dividing network, a level shifter, and a buffer. That is, it has structure which thought the cure against a hot carrier as important by forming a Lov field only between a channel formation field and a drain field, reducing a resistance component as much as possible. This is because the direction to which in the case of the above-mentioned circuit group the function of a source field and a drain field does not change to, but a carrier (electron) moves is fixed.
[0099] However, a Lov field can also be formed across a channel formation field if needed. That is, it is also possible to form between a source field and a channel formation field and between a drain field and a channel formation field.
[0100] Moreover, the n channel mold TFT303 fits the sampling circuit (it is also called the transfer gate) which thinks the both sides of the cure against a hot carrier, and low OFF state current actuation as important. That is, it considers as the cure against a hot carrier by forming a Lov field, and low OFF state current actuation is realized by forming a Loff field further. Moreover, since the function of a source field and a drain field is reversed and a sampling circuit changes the 180 degrees of the migration directions of a carrier, it must be made into structure which serves as axial symmetry centering on gate wiring. In addition, depending on the case, it can consider only as a Lov field.
[0101] Moreover, the n channel mold TFT304 fits the pixel section which thought low OFF state current actuation as important, and a sampling circuit. That is, low OFF state current actuation is realized by not arranging the Lov field which can become the factor which makes an OFF state current value increase, but arranging a Loff field and an offset field. Moreover, using the LDD field of concentration lower than the LDD field of a drive circuit as a Loff field has struck the cure which reduces an OFF state current value thoroughly, even if an ON state current value falls somewhat. Furthermore, it is checked that n mold impurity range (a) 221 is very effective when reducing an OFF state current value.
[0102] Moreover, what is necessary is just to set typically the 0.3-3.0 micrometers (width of face) of the die length of the Lov field 207 of the n channel mold TFT302 to 0.5-1.5 micrometers to 3-7 micrometers of channel length. Moreover, the die length (width of face) of the Lov fields 211a and 212a of the n channel mold TFT303 should just set typically the 0.3-3.0 micrometers (width of face) of the 1.0-3.5 micrometers of the die length of 0, 5-1.5 micrometers, and the Loff fields 211b and 212b to 1.5-2.0 micrometers. Moreover, what is necessary is just to set typically to 2.0-2.5 micrometers the 0.5-3.5 micrometers (width of face) of the die length of the Loff fields 217-220 established in a pixel TFT304.
[0103] Furthermore, the p channel mold TFT301 is formed in self align (self aryne), and the point that the n channel molds 302-TFT 304 are formed in nonself adjustment (non self aryne) is also one of the descriptions of this invention.
[0104] Moreover, at this example, occupancy area of retention volume required in order that specific inductive capacity may form a required capacity by having used 7-9, and the high alumina film as a dielectric of retention volume can be lessened. Furthermore, the numerical aperture of the image display section of an active matrix liquid crystal display can be raised by using as one electrode of retention volume the screen formed on Pixel TFT like this example.
[0105] In addition, this invention does not need to be limited to the structure of the retention volume shown in this example. For example, the retention volume of the structure indicated by the Japanese-Patent-Application-No. No. 316567 [nine to] application by these people, Japanese-Patent-Application-No. No. 273444 [nine to] application, or Japanese-Patent-Application-No. No. 254097 [ten to] application can also be used.
[0106] The process which produces an active matrix liquid crystal display is explained from a active-matrix substrate here. As shown in drawing 5 , the orientation film 501 is formed to the substrate of the condition of drawing 4 (B). In this example, the polyimide film is used as orientation film. Moreover, the counterelectrode 503 which consists of transparence electric conduction film, and the orientation film 504 are formed in the opposite substrate 502. In addition, a color filter and a screen may be formed in an opposite substrate if needed.

[0107] Next, after forming the orientation film, it adjusts so that orientation may be carried out with the fixed pre tilt angle which performs rubbing processing and has a liquid crystal molecule. And the pixel section, and the active-matrix substrate and opposite substrate with which the drive circuit was formed are stuck and set through a sealant, a spacer (not shown [both]), etc. according to a well-known cel **** process. Then, liquid crystal 505 is poured in among both substrates, and it closes completely with encapsulant (not shown). What is necessary is just to use a well-known liquid crystal ingredient for liquid crystal. Thus, the active matrix liquid crystal display shown in drawing 5 is completed.
[0108] Next, the configuration of this active matrix liquid crystal display is explained using the perspective view of drawing 8 . In addition, since drawing 8 matches with cross-section structural drawing of drawing 1 - drawing 4 , the common sign is used for it. A active-matrix substrate consists of the pixel section 801 formed on the quartz substrate 101, a scan (gate) signal drive circuit 802, and an image (source) signal drive circuit 803. The pixel TFT304 of the pixel section is the n channel mold TFT, and the drive circuit prepared on the outskirts is constituted on the basis of the CMOS circuit. The scan signal drive circuit 802 and the picture signal drive circuit 803 are connected to the pixel section 801 with the gate wiring 128 and source wiring 154, respectively. Moreover, the terminal 805 to which FPC804 was connected, and the drive circuit are electrically connected by the connection wiring 806 and 807.
[0109] Next, an example of the circuitry of the active matrix liquid crystal display shown in drawing 8 is shown in drawing 9 . this example -- an active matrix liquid crystal -- a display -- a picture signal -- a drive -- a circuit -- 901 -- a scan -- a signal -- a drive -- a circuit -- (-- A --) -- 907 -- a scan -- a signal -- a drive -- a circuit -- (-- B --) -- 911 -- precharge -- a circuit -- 912 -- a pixel -- the section -- 906 -- having -- **** . In addition, the picture signal processing circuit 901 and the scan signal drive circuit 907 are included in this specification in a drive circuit.
[0110] The picture signal drive circuit 901 is equipped with the shift register 902, the level shifter 903, the buffer 904, and the sampling circuit 905. Moreover, the scan signal drive circuit (A) 907 is equipped with the shift register 908, the level shifter 909, and the buffer 910. The scan signal drive circuit (B) 911 is also the same configuration.
[0111] As for shift registers 902 and 908, the structure by which, as for the n channel mold TFT used for the CMOS circuit which are 3.5-16V (typically 5 V or 10 V), and forms a circuit, driver voltage is shown by 302 of drawing 4 (B) is suitable here.
[0112] Moreover, the CMOS circuit in which level shifters 903 and 909 and buffers 904 and 910 contain the n channel mold TFT302 of drawing 4 (B) like a shift register although driver voltage becomes high with 14-16V is suitable. In addition, it is effective to make gate wiring into multi-gate structures, such as double-gate structure and triple gate structure, when raising each circuit reliability.
[0113] Moreover, since a sampling circuit 905 needs to reduce an OFF state current value when a source field and a drain field are reversed although driver voltages are 14-16V, the CMOS circuit containing the n channel mold TFT303 of drawing 4 (B) is suitable. In addition, although only the n channel mold TFT is illustrated in drawing 4 (B), it comes [sink-] to be easy of a high current and is desirable, when actually forming a sampling circuit and it forms combining the n channel mold TFT and the p channel mold TFT.
[0114] Moreover, since an OFF state current value still lower than a sampling circuit 905 is required, considering as the structure which does not arrange a Lov field is desirable, and, as for the pixel section 906, it is desirable [driver voltages are 14-16V, and] to use the n channel mold TFT304 of drawing 4 (B) as a pixel TFT .
[0115] In the invention in this application, the biggest description is in the point that an offset field exists between the LDD field of Pixel TFT, and a channel formation field. That is explained using drawing 7 . Drawing 7 is the sectional view which expanded a part of pixel TFT in the condition of having finished even the process of drawing 3 (C).
[0116] When Pixel TFT is produced at the production process of this example, as shown in drawing 7 , the offset field 701 (or 702) exists between the LDD fields 220 (or 219) which become in the channel formation field 214 and n mold impurity range (c). The die length of this offset field 701 is mostly in

agreement with the thickness (thickness of the part by which thickness here is strictly formed in the side attachment wall of gate wiring) of the cap film 142.
[0117] However, it cannot be overemphasized that the die length of the offset field 701 becomes shorter than the thickness of the cap film 142 by the surroundings lump at the time of adding Lynn.
[0118] In the invention in this application, the die length of these offset fields 701 and 702 may be 0-200nm (preferably 20-100nm, still more preferably 30-70nm). This die length is controllable by adjusting the thickness of the cap film 142.
[0119] Thus, in the invention in this application, since two resistance fields, a LDD field and an offset field, are prepared to Pixel TFT, it is possible to make an OFF state current value into a very low value. That is, as the electrical potential difference between source-drains called it 14V and gate voltage called it -17.5V, when TFT is in an OFF state completely, the OFF state current value of 5 or less (preferably 1 or less pA) pAs can be attained.
[0120] In addition, the configuration of this example is easily realizable by producing TFT according to the process shown in drawing 1 -4. Moreover, although this example shows only the configuration of the pixel section and a drive circuit, if the production process of an example 1 is followed, it is also possible a signal dividing network, a subharmonics circuit, a D/A converter circuit, an operational amplifier circuit, a gamma correction circuit, and to form digital disposal circuits (for you to call it a logical circuit), such as a microprocessor circuit, on the same substrate further.
[0121] Thus, this invention can realize an electro-optic device including the drive circuit for controlling the pixel section and the pixel section on the same substrate, for example, the electro-optic device which possesses a drive circuit and the pixel section on the same substrate.
[0122] Moreover, if the process to drawing 2 (B) of this example is performed, the crystalline substance silicon film of the unique crystal structure which has a continuity in a crystal lattice will be formed. Just refer to the application of Japanese Patent Application No. No. 044659 [ten to] by these people, Japanese Patent Application No. No. 152316 [ten to], Japanese Patent Application No. No. 152308 [ten to], or Japanese Patent Application No. No. 152305 [ten to] for the detail about such crystalline substance silicon film. Hereafter, these people explain an outline about the description of the crystal structure investigated experimentally. In addition, this description is in agreement with the description of the semi-conductor layer which forms the barrier layer of TFT completed by this example.
[0123] The above-mentioned crystalline substance silicon film has two or more needlelike or crystal structures which rod-like crystals (it is hereafter written as a cylindrical crystal) gathered, and were located in a line, if it sees microscopically. This can be easily checked by observation by TEM (transmission electron microscopy).
[0124] Moreover, if electron diffraction and X ray (X-ray) diffraction are used, it can check that the front face (part which forms a channel) of the crystalline substance silicon film has {110} sides as an orientation side although the gap of some is included in the crystallographic axis. At this time, if it analyzes by electron diffraction, it can check that the diffraction mottle corresponding to {110} sides appears finely. Moreover, each spot can also check having distribution on a concentric circle.
[0125] Moreover, if the grain boundary which each cylindrical crystal touches and forms is observed by HR-TEM (high-resolution transmission electron microscopy), it can check that a continuity is in a crystal lattice in the grain boundary. This can be easily checked from the plaid observed being continuously connected in the grain boundary.
[0126] In addition, the continuity of the crystal lattice in the grain boundary originates in the grain boundary being a grain boundary called a "plane grain boundary." The definition of the plane grain boundary in this specification, "it is Characterization of High-Efficiency Cast-Si Solar Cell Wafers by MBICMeasurement.; it is "Planar boundary" indicated by Ryuichi Shimokawa and Yutaka Hayashi, Japanese Journal ofApplied Physics vol.27, No.5, pp.751-758, and 1988."
[0127] According to the above-mentioned paper, a twin crystal grain boundary, a special stacking fault, a special twist grain boundary, etc. are included in a plane grain boundary. This plane grain boundary has the description of being inactive electrically. That is, though it is the grain boundary, since it does not function as a trap which checks migration of a carrier, it can be considered that it does not exist

substantially.
[0128] When especially crystallographics axis (shaft perpendicular to the crystal face) are <110> shafts, a {211} twin-crystal grain boundary is also called the coincidence boundary of sigma 3. sigma value is a parameter used as the guide in which extent of the adjustment of a coincidence boundary is shown, and it is known that it is a grain boundary with sufficient adjustment, so that sigma value is small.
[0129] If TEM is used and the crystalline substance silicon film of this example is observed in a detail, most grain boundaries (90% or more, typically 95% or more) are actually known by the coincidence boundary of sigma 3, and that it is a {211} twin-crystal grain boundary typically.
[0130] In the grain boundary formed between two crystal grain, if the angle which the plaid corresponding to {111} sides makes is set to theta when field bearing of both crystals is {110}, becoming the coincidence boundary of sigma 3 at the time of theta= 70.5 degrees is known. The crystalline substance silicon film of this example is continuing at the include angle each plaid of whose of the crystal grain which adjoins in the grain boundary is just about 70.5 degrees, and it can be said from that that this grain boundary is a coincidence boundary of sigma 3.
[0131] In addition, although it becomes the coincidence boundary of sigma 9 at the time of theta= 38.9 **, such other coincidence boundaries exist. Anyway, there is no change in being inactive.
[0132] It is shown that two different crystal grain in the grain boundary has joined such the crystal structure (correctly structure of the grain boundary) with very sufficient adjustment. That is, in the grain boundary, a crystal lattice stands in a row continuously, and has composition which cannot make the trap level resulting from a crystal defect etc. very easily. Therefore, the grain boundary does not exist substantially and the semi-conductor thin film which has such the crystal structure can be regarded.
[0133] Furthermore, it is checked by TEM observation that the defect which exists in crystal grain according to the heat treatment process (it is equivalent to the thermal oxidation process in an example 1) in the high temperature of 800-1150 degrees C is almost extinguished. This is clear also from the number of defects being sharply reduced before and behind this heat treatment process.
[0134] By electron-spin-resonance analysis (Electron Spin Resonance:ESR), the difference of this number of defects turns into a difference of spin density, and appears. In the present condition, the spin density of the crystalline substance silicon film of this example is . It has become clear that it is three or less (preferably three or less 3x1017 spins/cm) 5x1017 spins/cm. However, since this measured value is close to the limit of detection of an existing measuring device, it is expected that actual spin density is still lower.
[0135] Since it can consider that the crystalline substance silicon film of this example has extremely few defects in crystal grain, and the grain boundary does not exist substantially from the above thing, you may consider the single-crystal-silicon film or the substantial single-crystal-silicon film.
[0136] [Example 2] this example explains the configuration of the pixel section which has the structure shown in the example 1 using drawing 10 . In addition, in the plan shown in drawing 10 , the sign used in the example 1 is quoted as it is paying attention to 1 pixel of the arbitration of the pixel section.
[0137] Drawing 10 (A) is the plan showing superposition of a barrier layer, gate wiring, and source wiring, and this drawing (B) is a plan showing the condition of having piled up the screen and the pixel electrode on it. In drawing 10 (A), the gate wiring 128 intersects the barrier layer 114 under it through the gate dielectric film which is not illustrated. Moreover, although illustration has not been carried out, the Loff field which becomes in a source field, a drain field, and n mold impurity range (c) is formed in the barrier layer 114. Moreover, 1001 is the contact section of source wiring 154 and a barrier layer 114, and 1002 is the contact section of the drain wiring 157 and a barrier layer 114.
[0138] Moreover, in drawing 10 (B), the pixel electrodes 162 and 163 prepared for every pixel are formed on Pixel TFT with the screen 160 by which the anodic oxidation object (the anodic oxidation object 161 of drawing 4 (B) is pointed out although not illustrated here) was formed in the front face. And retention volume 164 is formed in the field with which a screen 160 and the pixel electrode 162 lap through an anodic oxidation object. In addition, 1003 is the contact section of the drain wiring 157 and the pixel electrode 162.
[0139] In this example, it is possible to lessen area for forming the capacity which needs specific

inductive capacity by using 7-9, and the high alumina film as a dielectric of retention volume. Furthermore, the numerical aperture of the image display section of an active matrix liquid crystal display can be raised by using as one electrode of retention volume the light-shielding film formed on Pixel TFT like this example.

[0140] [Example 3] this example explains the configuration of the pixel section using drawing 11 about the case where it shall differ in an example 2 (refer to drawing 10). In addition, the structure of the pixel section explained in the examples 1 and 2 is the same structure altogether only by some gate wiring differing. Therefore, explanation is given about the same part or the same sign is used.

[0141] Drawing 11 (A) is the sectional view of the pixel section of this example, and the description is that carries out the laminating of the 1st electric conduction film 1102, the 2nd electric conduction film 1103, and the 3rd electric conduction film 1104, and it forms the gate wiring (however, the part which laps with a barrier layer is removed) 1101. That is, the structure which sandwiched the 3rd electric conduction film 1104 by the 1st electric conduction film 1102 and the 2nd electric conduction film 1103 is taken.

[0142] In this example, the alloy film which uses aluminum as a principal component as the tantalum film and the 3rd electric conduction film 1104 as the tantalum nitride film and the 2nd electric conduction film 1103 as the 1st electric conduction film 1102 is used. In order to form this structure, the 1st electric conduction film 1102 is first formed on gate dielectric film, and the 3rd electric conduction film 1104 is formed on it. And patterning of the 3rd electric conduction film 1104 is carried out to a predetermined configuration, and a it top is covered by the 2nd electric conduction film 1103. Then, gate wiring of structure as etched the 1st electric conduction film 1102 and the 2nd electric conduction film 1103 by package and shown in drawing 11 (A) is formed.

[0143] It seems that and the plan at this time is shown in drawing 11 (B). That is, the parts (you may also call this part a gate electrode) 1105a and 1105b (it is equivalent to the gate wiring 128a and 128b of drawing 2 (E), respectively) which lap with a barrier layer among gate wiring become by the laminated structure of the 1st and 2nd electric conduction film. On the other hand, the gate wiring 1101 has wiring width of face thicker than the gate wiring 1105a and 1105b, and is formed by 3 layer structures as shown in drawing 11 (A). That is, in order to make wiring resistance small as much as possible, as for the part only used as wiring also in gate wiring, considering as structure like this example is desirable.

[0144] Moreover, as for the connection wiring 806 and 807 which connects a terminal 805, the scan signal drive circuit 802, and the picture signal drive circuit 803, in the active matrix liquid crystal display shown in drawing 8 of an example 1, it is desirable to attain low resistance-ization of wiring by using wiring of 3 layer structures which was explained by this example.

[0145] In addition, the structure shown in drawing 11 (B) is realizable by combining the formation approach of wiring structure explained by the example 1 and this example. Therefore, it is possible to combine the configuration of this example with the active matrix liquid crystal display explained in the example 1.

[0146] [Example 4] this example explains the pixel section of different structure from an example 1 using drawing 12 . In addition, since it is the structure as the pixel section shown in drawing 3 (C) where fundamental structure is the same, only difference is explained.

[0147] First, the structure of drawing 12 (A) is the example in which the buffer layer 1201 was formed between the 3rd interlayer insulation film 159 and a screen 160. As a buffer layer 1201, the insulator layer containing the silicon of 10-100nm (preferably 30-50nm) thickness is used. However, since degasifying out of the resin film will pose a problem if it puts to a vacuum when the 3rd interlayer insulation film 159 is organic resin film, it is desirable to use the insulator layer which can be formed by the spatter.

[0148] In this example, the silicon oxide film of 50nm thickness is used as a buffer layer 1201. By forming this buffer layer, the adhesion of the 3rd interlayer insulation film 159 and a screen 160 improves. In case an oxide 161 is formed with an anode oxidation method like an example 1, if adhesion is bad, the fault in which an anodic oxidation object is formed as hidden in the interface of the 3rd interlayer insulation film and a screen will occur. However, such fault can be prevented by considering

as the structure of drawing 12 (A).
[0149] Moreover, the structure of drawing 12 (B) is an example which forms a buffer layer 1202 in the bottom of a screen 160 in self align, although basic structure is the same as that of drawing 12 (A). In this case, the structure of drawing 12 (B) is realizable by etching a buffer layer in self align by using a screen 160 as a mask.
[0150] An etching process may be performed immediately after forming a screen 160, and after forming an oxide 161, it may be performed. However, when the ingredient of a buffer layer 1202 and the ingredient of oxide 161 are etched by the same etchant, before forming oxide 161, it is desirable to perform an etching process.
[0151] Moreover, it is advantageous when opening a contact hole in the 3rd interlayer insulation film 159 by considering as the structure of drawing 12 (B). When the silicon oxide film etc. exists on the organic resin film, in case the organic resin film is etched, there is a possibility that the silicon oxide film may remain in the shape of a canopy top. Therefore, it is desirable to remove a buffer layer in the location which forms a contact hole beforehand like the structure of drawing 12 (B).
[0152] Moreover, the structure of drawing 12 (C) shows the example which forms the spacers 1203a-1203d which become by the insulator layer after forming a screen 160 and an oxide 161, and forms the pixel electrode 1204 after that. As a Spacers [1203a-1203d] ingredient, the organic resin film is desirable and it is desirable to use the polyimide which has especially photosensitivity, and an acrylic.
[0153] By considering as structure like drawing 12 (C), since the edge (edge section) of a screen 160 will be hidden with a spacer, what a screen and a pixel electrode short-circuit at the edge of a screen 160 can be prevented.
[0154] In addition, the configuration of this example only changed even formation of formation of the 3rd interlayer insulation film - a pixel electrode in the production process of an example 1, and its other processes are good at the same process as an example 1. Therefore, it is also possible to apply to the active matrix liquid crystal display shown in the example 1. Moreover, it is possible to combine with any configuration shown in examples 1-3 freely.
[0155] The retention volume prepared in each pixel of the [example 5] pixel section can form retention volume by what the electrode (it is a screen in the case of this invention) of the direction which is not connected to the pixel electrode is made into fixed potential for. In that case, it is desirable to set a screen as floating (condition isolated electrically) or common potential (middle potential of the picture signal sent as data).
[0156] So, this example explains a screen using drawing 13 about the connection method in the case of fixing to common potential. In addition, since basic structure is the same as that of the pixel section explained by drawing 4 (B), it explains to the same part using the same sign.
[0157] In drawing 13 (A), 304 is the pixel TFT (n channel mold TFT) produced like the example 1, and 160 is a screen which functions as one electrode of retention volume. The screen 1301 which extended on the outside of the pixel section has connected with the current supply line 1303 which gives common potential through the contact hole 1302 established in the 3rd interlayer insulation film 159 and the passivation film 158. What is necessary is just to form this current supply line 1303 in source wiring or drain wiring, and coincidence.
[0158] Thus, on the outside of the pixel section, a screen 160 can be held to common potential by connecting electrically a screen 1301 and the current supply line 1303 which gives common potential. Therefore, before forming a screen 1301 in this case, the process which etches the 3rd interlayer insulation film 159 and the passivation film 158, and forms the contact hole is needed.
[0159] Next, in drawing 13 (B), 304 is the pixel TFT produced like the example 1, and 160 is a screen which functions as one electrode of retention volume. The screen 1304 which extended laps with the electric conduction film 1306 through an oxide 1307 in the field shown by 1305 to the outside of the pixel section. This electric conduction film 1306 is formed in the pixel electrode 162 and coincidence.
[0160] And this electric conduction film 1306 is connected with the current supply line 1309 which gives common potential through the contact hole 1308 established in the 3rd interlayer insulation film 159 and the passivation film 158. At this time, the capacitor which becomes by the screen 1304, oxide

1307, and the electric conduction film 1306 is formed in a field 1305. When the capacity of this capacitor is large enough (about 10 times of the sum total capacity of the total retention volume connected to all the pixels for 1 scan line), potential fluctuation of screens 1304 and 160 can be reduced by the electrostatic coupling formed in the field 1305.
[0161] Moreover, when adopting the structure of drawing 13 (B), it is desirable to adopt a source line reversal drive as the drive approach of an active matrix liquid crystal display. Since the electrical-potential-difference polarity impressed to a pixel electrode will be reversed for every frame if it is a source line reversal drive, if it equalizes in time, most amounts of charges accumulated in a screen 160 will serve as zero. That is, since the condition that potential fluctuation is very small is maintainable, the stable retention volume can be formed.
[0162] Thus, by adopting the structure of drawing 13 (B), it becomes possible to hold a screen to common potential, without increasing a routing counter.
[0163] In addition, the configuration of this example can realize the production process of an example 1 only by carrying out a partial change, and its other processes are good at the same process as an example 1. Therefore, it is also possible to apply to the active matrix liquid crystal display shown in the example 1. Moreover, it is possible to combine with any configuration shown in examples 1-3 freely.
[0164] Although the [example 6] example 1 showed the example which carries out gettering of the nickel used in order to crystallize the amorphous silicon film using Lynn, this example explains the case where gettering of the above-mentioned catalyst element is carried out using other elements.
[0165] First, the semi-conductor film (this example crystalline substance silicon film) which has the crystal structure according to the process of an example 1 (to the process of drawing 1 (B)) is obtained. However, let introductory concentration of the catalyst element (nickel is taken for an example) used for crystallization be a low thing as much as possible in this example. A 0.5-3 ppm nickel content layer is formed by weight conversion on the amorphous silicon film, and, specifically, heat treatment for crystallization is performed. The nickel concentration contained in the crystalline substance silicon film formed by this serves as 1x1017 - 1x1019 atoms/cm3 (typically 5x1017 - 1x1018 atoms/cm3).
[0166] And if the crystalline substance silicon film is formed, after removing the mask film, it will heat-treat in the oxidizing atmosphere containing a halogen. Temperature is made into 800-1150 degrees C (preferably 900-1000 degrees C), and the processing time is made into 10 minutes - 4 hours (preferably 30 minutes - 2 hours).
[0167] In this example, 950-degree-C heat treatment for 30 minutes is performed into the ambient atmosphere in which the hydrogen chloride of 3 - 10 volume % was included [be / it / under / oxygen ambient atmosphere / receiving]. The nickel in the crystalline substance silicon film serves as an volatile chlorination compound (nickel chloride) according to this process, and it breaks away in a processing ambient atmosphere. That is, it becomes possible to remove nickel according to a gettering operation of a halogen. However, if the nickel concentration which exists in the crystalline substance silicon film is too high, the problem that oxidation advances unusually in the segregation section of nickel will be produced. Therefore, it is necessary to make low concentration of the nickel used in the phase of crystallization as much as possible.
[0168] in this way, the concentration of the nickel which is alike and remains in the formed crystalline substance silicon film serves as 1x1016 atms/cm3 preferably three or less 1x1017 atms/cm. What is necessary is after this, just to carry out the process after drawing 1 (D) according to an example 1.
[0169] In addition, it is also possible to apply the configuration of this example to an example 1, and it is also possible to apply to the active matrix liquid crystal display shown in the example 1. Moreover, it is possible to combine with any configuration of examples 2-5 freely. Moreover, it is also possible to use together with the gettering process by Lynn shown in the example 1.
[0170] [Example 7] this example shows the example using a different process from an example 1 about the formation approach of n mold impurity range (c). Drawing 14 is used for explanation.
[0171] First, the condition of drawing 3 (B) is acquired according to the process of an example 1. Next, the resist masks 132-134 are removed and the cap film 142 is formed. Thickness of the cap film 142 is set to 20nm in this example.

[0172] Next, the semi-conductor film (not shown) is formed in the thickness of 0.8-1 micrometer, and Sidewalls 1401a and 1401b are formed by performing anisotropic etching. And n mold impurity element is added like drawing 3 (C) in this condition, and n mold (impurity range c) 1402a and 1402b are formed. Since Sidewalls 1401a and 1401b also function as a mask at this time, the offset fields 1403a and 1403b are formed.
[0173] In this example, the die length (width of face) of the offset fields 1403a and 1403b is determined by the thickness of Sidewalls 1401a and 1401b and the cap film 142. This example is effective to form for a long time, as it said especially that an offset field was 100-200nm.
[0174] Although the die length of an offset field is determined by the thickness (thickness of the part formed in the side attachment wall of gate wiring) of the cap film 142 in the example 1, for realizing die length of 100-200nm, thickness of the cap film 142 must also be thickened according to it. However, since n mold impurity range (c) adds n mold impurity element through the cascade screen of gate dielectric film and the cap film, if thickness of gate dielectric film is not made extremely thin, the throughput of an impurity addition process will be reduced sharply.
[0175] Therefore, if it is a configuration like this example, the die length of the offset fields 1403a and 1403b can be substantially decided by Sidewalls 1401a and 1401b, and can be decided regardless of the thickness of gate dielectric film. In addition, in this example, in case Sidewalls 1401a and 1401b are formed, the cap film 142 is formed in order to secure etch selectivity, but as long as there is no need, you may omit.
[0176] In addition, the configuration of this example can also be combined with an example 1, and can also be applied to the active matrix liquid crystal display shown in the example 1. Moreover, it is possible to combine with any configuration of examples 2-5 freely.
[0177] [Example 8] this example explains the example in the case of producing a active-matrix substrate at a different process from an example 1.
[0178] In the example 1, the impurity element which gives one conductivity type by through doping whose formation process of p mold impurity range (a) and formation process of n mold impurity range (a) minded gate dielectric film is added. However, in case these impurity ranges are formed, where it removed gate dielectric film and a barrier layer is exposed, you may carry out.
[0179] In this case, if it advances to the process of drawing 2 (E) according to the process of an example 1, gate dielectric film will be etched in self align by using gate wiring 125-128 as a mask, and a part of barrier layers 111-114 will be exposed. In addition, an etching process can be performed at this time, without leaving the resist mask (not shown) used at the time of formation of gate wiring as it is, and giving a damage to a mask, then gate wiring.
[0180] What is necessary is after this, just to carry out sequential formation of p mold impurity range (a) and the n mold impurity range (a) like the example 1. However, unlike an example 1, since the addition conditions of an impurity element do not need to let gate dielectric film pass, they set up acceleration voltage low. An operation person should just choose the optimal conditions so that high impurity concentration contained about addition conditions in p mold impurity range (a) and n mold impurity range (a) may be realized.
[0181] When the production process of this example is adopted, the process equivalent to drawing 3 (C) of an example 1 comes to be shown in drawing 15 (A). In drawing 15 (A), it is gate dielectric film which 1501-1505 used gate wiring as the mask, and was formed in self align, and gate wiring is covered and the cap film 1506 is formed. And n mold impurity element is added like drawing 3 (c) in this condition, and n mold (impurity range c) 1507-1510 are formed. At this time, the offset field (not shown) of the die length which is mostly equivalent to the thickness of the cap film 1506 is formed between the channel formation fields 1511 and 1512 and n mold (impurity range c) 1507-1510.
[0182] Moreover, as shown in drawing 15 (B) depending on the case, the laminating of the 2nd cap film 1513 may be further carried out on the cap film 1506, and n mold impurity element may be added through the cascade screen. n mold impurity range (c) formed by this Between 1514-1517, and the channel formation fields 1518 and 1519, the offset field (not shown) of the die length which is mostly equivalent to the sum total thickness of the cap film 1506 and the 2nd cap film 1513 is formed.

[0183] With the configuration of drawing 15 (B), the die length of an offset field can be freely adjusted by adjusting the thickness of the 2nd cap film 1513. the insulator layer (preferably nitriding silicon oxide film) in which the 2nd cap film 1513 contains silicon -- using -- thickness -- 30-200nm (preferably 50-150nm) -- then, it is good.
[0184] Although the silicon nitride film is used as cap film (the 1st cap film) 1506 in this example, when a silicon nitride film is attached thickly, it has a possibility of stress becoming strong and producing faults, such as film peeling. Therefore, although he wants to form in a certain amount of thickness as antioxidizing film of gate wiring, if thickness is thin, an effective offset field may be unable to be formed. When such, the configuration shown in drawing 15 (B) is effective.
[0185] In addition, it can realize, if an example 1 is transformed, and the configuration of this example can also be applied to the active matrix liquid crystal display shown in the example 1. Moreover, it is possible to combine with any configuration of examples 2-7 freely.
[0186] At [example 9] this example, a different process from an example 1 explains the example in the case of producing a active-matrix substrate using drawing 16 .
[0187] First, according to the process of an example 1, it carries out to the process of drawing 2 (E). Next, the cap film (this example nitriding silicon oxide film) 1601 which becomes with the same ingredient as gate dielectric film is formed in the thickness of 30nm. And the addition process of an N type impurity element is performed on the same conditions as drawing 3 (C), and n mold (impurity range c) 1602-1603 are formed. (Drawing 16 (A))
[0188] Next, gate dielectric film is etched in self align by using gate wiring as a mask, and gate dielectric film 1605-1609 is formed directly under gate wiring. next, the resist mask 1610 -- forming -- drawing 3 (A) -- the same -- the addition process of p mold impurity element -- carrying out -- p mold impurity range (a) -- 1611 and 1612 are formed. (Drawing 16 (B))
[0189] Next, the resist mask 1610 is removed and the resist masks 1613-1616 are newly formed. And the addition process of n mold impurity element is performed like drawing 3 (B), and n mold (impurity range a) 1617-1623 are formed. (Drawing 16 (C))
[0190] Next, the resist masks 1613-1616 are removed and the 1st interlayer insulation film 1624 is formed. Although the cascade screen of the silicon nitride film of 50nm thickness and the nitriding silicon oxide film of 200nm thickness is used in this example, it is possible not only multilayer structure but to use the monolayer structure which becomes by the insulator layer containing silicon.
[0191] Next, the activation process of the impurity element added after forming the 1st interlayer insulation film 1624 is performed. In this example, it is activated by furnace annealing of 800-degree-C 1 hour. (Drawing 16 (D))
[0192] According to the above production processes, a active-matrix substrate is produced, a well-known cel **** process can be performed and an active matrix liquid crystal display can be produced. In addition, a structurally different point from the active-matrix substrate (drawing 4 (B)) shown in the example 1 is only the configuration of gate dielectric film and the 1st interlayer insulation film, and what the function of a drive circuit and the pixel section does not change to an example 1 is obtained.
[0193] In addition, it is also possible to produce an active matrix liquid crystal indicating equipment equivalent to the active matrix liquid crystal indicating equipment which could realize the configuration of this example when changing the applicable part of an example 1, and was shown in the example 1. Moreover, it is possible to combine with any configuration of examples 2-8 freely.
[0194] In the production process shown in the [example 10] example 1, although the example which performs a channel dope process only to the field used as the n channel mold TFT, and controls a threshold electrical potential difference is shown, it is also possible to perform a channel dope process without distinction of the n channel mold TFT or the p channel mold TFT on the whole surface. In that case, since the number of photo masks of a production process becomes fewer, the throughput of a process and improvement in the yield can be aimed at.
[0195] Moreover, a channel dope process is given to the whole surface depending on the case, and the impurity element which gives a conductivity type contrary to the impurity element added on the whole surface in either the n channel mold TFT or the p channel mold TFT can be added.

[0196] In addition, the configuration of this example can be freely combined with any configuration shown in examples 2-9.
[0197] In the example of a production process shown in the [example 11] example 1, before forming gate wiring of the n channel mold TFT, it is the requisite to form n mold impurity range (b) which functions as a Lov field later beforehand. And it has been the description that p mold impurity range (a) and n mold impurity range (c) are formed in both self align.
[0198] However, in order to acquire the effectiveness of this invention, it is not limited to the process which results there that final structure should just be structure like drawing 4 (B). Therefore, an operation person may change the formation sequence of an impurity range suitably. Moreover, it is also possible to form p mold impurity range (a) and n mold impurity range (c) using a resist mask depending on the case. That is, as finally shown in drawing 4 (B), as long as TFT which has the barrier layer of a configuration of differing according to each circuit is formed, the process sequence of all combination may be adopted.
[0199] [Example 12] this example explains the case where this invention is applied to the semiconductor device produced on the silicon substrate. Typically, it is applicable to the reflective mold liquid crystal display using a metal membrane with a reflection factor high as a pixel electrode.
[0200] This example adds n mold or p mold impurity element directly to a silicon substrate (silicon wafer) in an example 1, and forms impurity ranges, such as a LDD field, a source field, or a drain field. Neither the formation sequence of each impurity range nor the formation sequence of gate dielectric film is asked in that case.
[0201] In addition, the configuration of this example can be freely combined with any configuration of examples 1-11. However, since it is decided that the semi-conductor layer used as a barrier layer will be a single crystal silicon substrate, it serves as combination other than a crystallization process.
[0202] although the [example 13] example 1 explained on the assumption that a Lov field and a Loff field were arranged only in the n channel mold TFT and the location was properly used according to a circuit specification -- TFT size -- small -- becoming (channel length becoming short) -- the same thing can be said now also to the p channel mold TFT.
[0203] That is, if channel length is set to 2 micrometers or less, in order for a short channel effect to actualize, the need of arranging a Lov field also in the p channel mold TFT depending on the case comes out. Thus, in this invention, the p channel mold TFT may not be limited to the structure shown in examples 1, 4-31, and may be the same structure as the n channel mold TFT.
[0204] In addition, what is necessary is just to form the impurity range where p mold impurity element is contained by 2x1016 - 5x1019 atoms/cm3 like formation of n mold impurity range (b) in the configuration of an example 1, when carrying out this example. Moreover, the configuration of this example can be freely combined with any configuration of examples 2-13.
[0205] It is also possible to use, in case [example 14] this invention forms an interlayer insulation film on the conventional MOSFET and TFT is formed on it. That is, it is also possible to realize the semiconductor device of the three-dimensional structure. Moreover, it is also possible to use SOI substrates, such as SIMOX, Smart-Cut (trademark of SOITEC), and ELTRAN (trademark of canon incorporated company), as a substrate.
[0206] In addition, the configuration of this example can be freely combined with any configuration of examples 1-12.
[0207] The liquid crystal display produced by [example 15] this invention can use various liquid crystal ingredients. As such an ingredient, the mixture (antiferroelectricity liquid crystal mixture) of TN liquid crystal, PDLC (polymer distributed liquid crystal) and FLC (ferroelectric liquid crystal), AFLC (anti-**********) or FLC, and AFLC is mentioned.
[0208] For example "H. Furue et al.;Charakteristics and Drivng Scheme of Polymer-Stabilized Monostable FLCD Exhibiting Fast Response Time and High Contrast Ratio with Gray-Scale Capability, SID, 1998", "T. Yoshida et al.;A Full-Color Thresholdless Antiferroelectric LCDExhibiting Wide Viewing Angle with Fast Response Time, 841, SID97DIGEST, 1997", "S. Inui et al.;Thresholdless antiferroelectricity in liquid crystals and its application to displays, 671-673, J.Mater.Chem.6(4), The

ingredient indicated by 1996" or U.S. Pat. No. 5,594,569 can be used.
[0209] what shows the electro-optics response characteristic of a V character mold (or U character mold) to the non-threshold antiferroelectricity liquid crystal mixture (it is written as Thresholdless Antiferroelectric LCD:TL-AFLC) in which the electro-optics response characteristic from which permeability changes continuously to electric field especially is shown -- it is -- the driver voltage -- about -- the about [**2.5V] (about 1 micrometer - 2 micrometers of cel thickness) thing is also found out. Therefore, possibility of the supply voltage for the pixel sections being managed with about 5-8V, and operating a drive circuit and the pixel section with the same supply voltage is suggested. That is, low-power-ization of the whole liquid crystal display can be attained.
[0210] Moreover, a ferroelectric liquid crystal and antiferroelectricity liquid crystal have the advantage that a speed of response is quick compared with TN liquid crystal. Since TFT which is used by this invention can realize TFT with a very quick working speed, it can realize a liquid crystal display with the quick image speed of response which fully employed the speed of the speed of response of a ferroelectric liquid crystal or antiferroelectricity liquid crystal efficiently.
[0211] Moreover, generally, non-threshold antiferroelectricity liquid crystal mixture has large spontaneous polarization, and its dielectric constant of the liquid crystal itself is high. For this reason, in using non-threshold antiferroelectricity liquid crystal mixture for a liquid crystal display, comparatively big retention volume is needed for a pixel. Therefore, it is desirable to use non-threshold antiferroelectricity liquid crystal mixture with small spontaneous polarization. Since the retention volume shown by drawing 3 (C) of an example 1 in such semantics can accumulate a big capacity in a small area, it is desirable.
[0212] In addition, it cannot be overemphasized that it is effective to use the liquid crystal display of this example as a display display of electronic equipment, such as a personal computer.
[0213] Moreover, the configuration of this example can be freely combined with any configuration of examples 1-14.
[0214] The [example 16] invention in this application can also be applied to a active-matrix mold EL (electroluminescence) display (it is also called a active-matrix mold EL display). The example is shown in drawing 17 .
[0215] Drawing 17 is the circuit diagram of the active-matrix mold EL display of this example. 81 expresses the viewing area and the direction (source side) drive circuit 82 of X and the direction (gate side) drive circuit 83 of Y are formed around it. Moreover, each pixel of a viewing area 81 has TFT84 for switching, a capacitor 85, TFT86 for current control, and EL element 87, and direction signal-line of X (source signal line) 88a (or 88b) and direction signal-line (gate signal line) of Y 89a (or 89b, 89c) are connected to TFT84 for switching. Moreover, the power-source lines 90a and 90b are connected to TFT86 for current control.
[0216] In the active-matrix mold EL display of this example, the X directional control circuit 82 and the Y directional control circuit 83 are formed in the p channel mold TFT301 list of drawing 4 (B) combining the n channel mold TFT302 or 303. Moreover, the p channel mold TFT301 of drawing 4 (B) is used for TFT86 for current control at TFT84 for switching using the n channel mold TFT304 of drawing 4 (B). Of course, it is not necessary to limit the combination of TFT to this.
[0217] In addition, which configuration of examples 1-13 may be combined to the active-matrix mold EL display of this example.
[0218] [Example 17] this example explains the example which produced EL (electroluminescence) display using the invention in this application. In addition, drawing 18 (A) is the plan of EL display of the invention in this application, and drawing 18 (B) is the sectional view.
[0219] In drawing 18 (A), for 4001, as for the pixel section and 4003, a substrate and 4002 are [a source side drive circuit and 4004] gate side drive circuits, and each drive circuit results in FPC (flexible print circuit)4006 through wiring 4005, and is connected to an external instrument.
[0220] At this time, as the pixel section 4002, the source side drive circuit 4003, and the gate side drive circuit 4004 are surrounded, the 1st sealant 4101, the covering material 4102, a filler 4103, and the 2nd sealant 4104 are formed.

[0221] Moreover, drawing 18 (B) is equivalent to the sectional view which cut drawing 18 (A) by A-A', and TFT4202 for current control (TFT which controls the current to an EL element) contained in the drive TFT(however, n channel mold TFT and p channel mold TFT are illustrated here.) 4201 and the pixel section 4002 which are contained in the source side drive circuit 4003 is formed on the substrate 4001.
[0222] In this example, TFT of the same structure as the p channel mold TFT301 of drawing 4 (B) and the n channel mold TFT302 is used for drive TFT4201, and TFT of the same structure as the p channel mold TFT301 of drawing 4 (B) is used for TFT4202 for current control. Moreover, the retention volume (not shown) connected to the gate of TFT4202 for current control is prepared in the pixel section 4002.
[0223] On drive TFT4201 and a pixel TFT4202, the interlayer insulation film (flattening film) 4301 which becomes with a resin ingredient is formed, and the pixel electrode (anode plate) 4302 electrically connected with the drain of a pixel TFT4202 is formed on it. As a pixel electrode 4302, the large transparence electric conduction film of a work function is used. As transparence electric conduction film, the compound of indium oxide and the tin oxide or the compound of indium oxide and a zinc oxide can be used.
[0224] And an insulator layer 4303 is formed on the pixel electrode 4302, and, as for the insulator layer 4303, opening is formed on the pixel electrode 4302. In this opening, the EL (electroluminescence) layer 4304 is formed on the pixel electrode 4302. The EL layer 4304 can use a well-known organic electroluminescence ingredient or inorganic EL ingredient. Moreover, whichever may be used although there are a low-molecular system (monomer system) ingredient and a macromolecule system (polymer system) ingredient as organic electroluminescence ingredient.
[0225] The formation approach of the EL layer 4304 should just use a well-known vacuum evaporationo technique or the applying method technique. Moreover, what is necessary is just to make structure of EL layer into a laminated structure or monolayer structure, combining freely a hole-injection layer, an electron hole transportation layer, a luminous layer, an electronic transportation layer, or an electron injection layer.
[0226] On the EL layer 4304, the cathode 4305 which consists of electric conduction film (the electric conduction film which uses aluminum, copper, or silver as a principal component typically, or cascade screen of them and other electric conduction film) which has protection-from-light nature is formed. Moreover, as for the moisture which exists in the interface of cathode 4305 and the EL layer 4304, or oxygen, eliminating as much as possible is desirable. Therefore, the device of carrying out continuation membrane formation of both in a vacuum, or forming the EL layer 4304 in nitrogen or a rare-gas ambient atmosphere, and forming cathode 4305, making neither oxygen nor moisture touched is required. At this example, the above membrane formation is enabled by using the membrane formation equipment of a multi chamber method (cluster tool method).
[0227] And cathode 4305 is electrically connected to wiring 4005 in the field shown by 4306. Wiring 4005 is wiring for giving a predetermined electrical potential difference to cathode 4305, and is electrically connected to FPC4006 through the different direction conductivity film 4307.
[0228] The EL element which consists of the pixel electrode (anode plate) 4302, an EL layer 4304, and cathode 4305 as mentioned above is formed. This EL element is surrounded by the covering material 4102 stuck on the substrate 4001 by the 1st sealant 4101 and the 1st sealant 4101, and is enclosed by the filler 4103.
[0229] As covering material 4102, a glass plate, a metal plate (typically stainless plate), a ceramic plate, an FRP (Fiberglass-Reinforced Plastics) plate, a PVF (polyvinyl fluoride) film, a Mylar film, polyester film, or an acrylic film can be used. Moreover, the sheet of the structure which sandwiched aluminium foil with the PVF film or the Mylar film can also be used.
[0230] However, covering material must be transparent when the direction of a light emission from an EL element goes to a covering material side. In that case, transparence matter like a glass plate, a plastic sheet, polyester film, or an acrylic film is used.
[0231] Moreover, as a filler 4103, ultraviolet-rays hardening resin or heat-curing resin can be used, and PVC (polyvinyl chloride), an acrylic, polyimide, an epoxy resin, silicone resin, and PVB (polyvinyl

BUCHIRARU) or EVA (ethylene vinyl acetate) can be used. If the hygroscopic matter (preferably barium oxide) is prepared in the interior of this filler 4103, degradation of an EL element can be controlled.

[0232] Moreover, a spacer may be made to contain in a filler 4103. At this time, if a spacer is formed with the barium oxide, it is possible to give hygroscopicity to the spacer itself. Moreover, when a spacer is formed, it is also effective to prepare the resin film on cathode 4305 as a buffer layer which eases the pressure from a spacer.

[0233] Moreover, wiring 4005 is electrically connected to FPC4006 through the different direction conductivity film 4307. Wiring 4005 tells the signal sent to the pixel section 4002, the source side drive circuit 4003, and the gate side drive circuit 4004 to FPC4006, and is electrically connected with an external instrument by FPC4006.

[0234] Moreover, in this example, the 2nd sealant 4104 is formed so that the disclosure section of the 1st sealant 4101 and a part of FPC4006 may be covered, and it has structure which intercepts an EL element from the open air thoroughly. In this way, it becomes EL display which has the cross-section structure of drawing 18 (B). In addition, EL display of this example may be produced combining examples 1, 3, 6-11 and which 13 or 14 configurations.

[0235] Top-face structure is shown in drawing 20 (A), and a circuit diagram is shown for the still more detailed cross-section structure which is the pixel section in drawing 19 here at drawing 20 (B). What is necessary is just to refer to mutually in drawing 19 , drawing 20 (A), and drawing 20 (B), since a common sign is used.

[0236] In drawing 19 , TFT4402 for switching prepared on the substrate 4401 is formed using the n channel mold TFT304 of drawing 4 (B). Therefore, just refer to the explanation of the n channel mold TFT304 for explanation of structure. Moreover, wiring shown by 4403 is gate wiring which connects electrically the gate electrodes 4404a and 4404b of TFT4402 for switching.

[0237] In addition, although considered as the double-gate structure where two channel formation fields are formed, in this example, you may be the single gate structure or the triple gate structure formed three where one channel formation field is formed.

[0238] Moreover, the drain wiring 4405 of TFT4402 for switching is electrically connected to the gate electrode 4407 of TFT4406 for current control. In addition, TFT4406 for current control is formed using the p channel mold TFT301 of drawing 4 (B). Therefore, just refer to the explanation of the p channel mold TFT301 for explanation of structure. In addition, although considered as single gate structure in this example, you may be double-gate structure or triple gate structure.

[0239] The 1st passivation film 4408 is formed on TFT4402 for switching, and TFT4406 for current control, and the flattening film 4409 which consists of resin is formed on it. It is very important to carry out flattening of the level difference by TFT using the flattening film 4409. Since EL layer formed behind is very thin, poor luminescence may be caused when a level difference exists. Therefore, before forming a pixel electrode so that EL layer can be formed as much as possible in a flat side, it is desirable to carry out flattening.

[0240] Moreover, 4410 is a pixel electrode (anode plate of an EL element) which consists of transparence electric conduction film, and is electrically connected to the drain wiring 4411 of TFT4406 for current control. The electric conduction film which consists of a compound of indium oxide and the tin oxide or a compound of indium oxide and a zinc oxide as a pixel electrode 4410 can be used.

[0241] The EL layer 4412 is formed on the pixel electrode 4410. In addition, although only 1 pixel is illustrated in drawing 19 , EL layer corresponding to each color of R (red), G (green), and B (blue) is made and divided in this example. Moreover, in this example, the low-molecular system organic electroluminescence ingredient is formed with vacuum deposition. It is considering as the laminated structure which prepared the copper-phthalocyanine (CuPc) film of 20nm thickness as a hole-injection layer, and specifically prepared the tris-8-quinolinolato aluminum complex (Alq3) film of 70nm thickness as a luminous layer on it. The luminescent color is controllable by adding fluorochromes, such as Quinacridone, perylene, or DCM1, to Alq3.

[0242] However, the above example is an example of the organic electroluminescence ingredient which

can be used as an EL layer, and there is no need of limiting to this. What is necessary is just to form EL layer (layer for moving luminescence and the carrier for it), combining freely a luminous layer, a charge transportation layer, or a charge impregnation layer. For example, although this example showed the example which uses a low-molecular system organic electroluminescence ingredient as an EL layer, a macromolecule system organic electroluminescence ingredient may be used. Moreover, it is also possible to use inorganic materials, such as silicon carbide, as a charge transportation layer or a charge impregnation layer. These organic electroluminescence ingredients and inorganic materials can use a well-known ingredient.

[0243] Next, on the EL layer 4412, the cathode 4413 which consists of electric conduction film of protection-from-light nature is formed. In the case of this example, the alloy film of aluminum and a lithium is used as electric conduction film of protection-from-light nature. Of course, the well-known MgAg film (alloy film of magnesium and silver) may be used. What is necessary is just to use the electric conduction film which added the electric conduction film which consists of an element belonging to one group of a periodic table, or two groups as a cathode material, or those elements.

[0244] When formed to this cathode 4413, EL element 4414 is completed. In addition, EL element 4414 here points out the capacitor formed in the pixel electrode (anode plate) 4410, the EL layer 4412, and cathode 4413.

[0245] Next, the top-face structure of the pixel in this example is explained using drawing 20 (A). The source of TFT4402 for switching is connected to source wiring 4415, and a drain is connected to the drain wiring 4405. Moreover, the drain wiring 4405 is electrically connected to the gate electrode 4407 of TFT4406 for current control. Moreover, the source of TFT4406 for current control is electrically connected to the current supply source line 4416, and a drain is electrically connected to the drain wiring 4417. Moreover, the drain wiring 4417 is electrically connected to the pixel electrode (anode plate) 4418 shown by the dotted line.

[0246] Retention volume is formed in the field shown by 4419 at this time. Retention volume 4419 is formed between the insulator layer (not shown) of the same layer as the semi-conductor film 4420 and gate dielectric film which were electrically connected with the current supply source line 4416, and the gate electrode 4407. Moreover, the capacity formed by the same layer (not shown) as the gate electrode 4407 and the 1st interlayer insulation film and the current supply source line 4416 can also be used as retention volume.

[0247] In addition, in producing EL display of this example, examples 1, 3, 6-11 and 13 or 14 configurations may be combined freely.

[0248] [Example 18] this example explains EL display with pixel structure which is different in an example 17. Drawing 21 is used for explanation. In addition, what is necessary is just to refer to explanation of an example 17 about the part to which the same sign as drawing 19 is given.

[0249] In drawing 21 , TFT of the same structure as the n channel mold TFT302 of drawing 4 (B) is used as TFT4501 for current control. Of course, the gate electrode 4502 of TFT4501 for current control is connected to the drain wiring 4405 of TFT4402 for switching. Moreover, the drain wiring 4503 of TFT4501 for current control is electrically connected to the pixel electrode 4504.

[0250] In this example, the pixel electrode 4504 functions as cathode of an EL element, and forms using the electric conduction film of protection-from-light nature. What is necessary is just to specifically use the electric conduction film which added the electric conduction film which consists of an element belonging to one group of a periodic table, or two groups, or those elements, although the alloy film of aluminum and a lithium is used.

[0251] The EL layer 4505 is formed on the pixel electrode 4504. In addition, although only 1 pixel is illustrated in drawing 21 , EL layer corresponding to G (green) is formed by vacuum deposition and the applying method (preferably spin coating method) in this example. It is considering as the laminated structure which prepared the lithium fluoride (LiF) film of 20nm thickness as an electron injection layer, and specifically prepared the PPV (poly para-phenylene vinylene) film of 70nm thickness as a luminous layer on it.

[0252] Next, on the EL layer 4505, the anode plate 4506 which consists of transparence electric

conduction film is formed. In the case of this example, the electric conduction film which consists of a compound of indium oxide and the tin oxide or a compound of indium oxide and a zinc oxide as transparence electric conduction film is used.
[0253] When formed to this anode plate 4506, EL element 4507 is completed. In addition, EL element 4507 here points out the capacitor formed in the pixel electrode (cathode) 4504, the EL layer 4505, and cathode 4506.
[0254] At this time, it has very important semantics that TFT4501 for current control is the structure of the invention in this application. Since TFT4501 for current control is a component for controlling the amount of currents which flows EL element 4507, many currents flow and the danger of degradation by heat or degradation by the hot carrier is also a high component. Therefore, the structure of the invention in this application which forms the LDD field 4509 so that it may lap with the gate electrode 4502 through gate dielectric film 4508 at the drain side of TFT4501 for current control is very effective.
[0255] Moreover, TFT4501 for current control of this example forms the parasitic capacitance called gate capacitance between the gate electrode 4502 and the LDD field 4509. It is also possible to give a function equivalent to the retention volume 4418 shown in drawing 20 (A) and (B) by adjusting this gate capacitance. Since it is smaller than the case where the capacitance of retention volume makes it operate by the analog drive method and ends when operating EL indicating equipment by the digital drive method especially, gate capacitance can be substituted for retention volume.
[0256] In addition, in producing EL display of this example, examples 1, 3, 6-11 and 13 or 14 configurations may be combined freely.
[0257] [Example 19] this example shows the example of the pixel structure where it can use for the pixel section of EL display shown in the example 17 or the example 18 to drawing 22 (A) - (C). in addition, this example -- setting -- 4601 -- in gate wiring of TFT4602 for switching, and 4604, a capacitor, and 4606 and 4608 make it as a current supply source line, and 4607 makes TFT for current control, and 4605 an EL element for the source wiring of TFT4602 for switching, and 4603.
[0258] Drawing 22 (A) is an example at the time of making the current supply source line 4606 common between two pixels. That is, the description is formed so that two pixels may serve as axial symmetry focusing on the current supply source line 4606. In this case, since the number of a current supply line can be reduced, the pixel section can be further made highly minute.
[0259] Moreover, drawing 22 (B) is an example at the time of forming the current supply source line 4608 in parallel with the gate wiring 4603. In addition, although it has structure established so that the current supply source line 4608 and the gate wiring 4603 might not lap in drawing 22 (B), if it is wiring formed in the layer from which both differ, it can also prepare so that it may lap through an insulator layer. In this case, since the current supply line 4608 and the gate wiring 4603 can be made to share monopoly area, the pixel section can be further made highly minute.
[0260] Moreover, drawing 22 (C) forms the current supply source line 4608 in parallel with the gate wiring 4603 like the structure of drawing 22 (B), and the description is that it forms two pixels further so that it may become axial symmetry focusing on the current supply source line 4608. Moreover, it is also effective to form the current supply source line 4608 so that it may lap with either of the gate wiring 4603. In this case, since the number of a current supply line can be reduced, the pixel section can be further made highly minute.
[0261] [Example 20] The electro-optic device and semiconductor circuit of the invention in this application can be used as the display and digital disposal circuit of an electric appliance. As such an electric appliance, the picture reproducer equipped with a video camera, a digital camera, a projector, Projection TV, a goggles mold display (head mount display), a navigation system, a sound system, a note type personal computer, a game device, Personal Digital Assistants (a mobile computer, a cellular phone, a handheld game machine, or digital book), and a record medium etc. is mentioned. The example of these electric appliances is shown in drawing 23 -25.
[0262] Drawing 23 (A) is a cellular phone and consists of a body 2001, the voice output section 2002, the voice input section 2003, a display 2004, an actuation switch 2005, and an antenna 2006. The electro-optic device of the invention in this application can be used for a display 2004, and the

semiconductor circuit of the invention in this application can be used for the voice output section 2002, the voice input section 2003 or CPU, memory, etc.
[0263] Drawing 23 (B) is a video camera and consists of a body 2101, a display 2102, the voice input section 2103, an actuation switch 2104, a dc-battery 2105, and the television section 2106. The electro-optic device of the invention in this application can be used for a display 2102, and the semiconductor circuit of the invention in this application can be used for the voice input section 2103 or CPU, memory, etc.
[0264] Drawing 23 (C) is a mobile computer (Mobile computer), and consists of a body 2201, the camera section 2202, the television section 2203, an actuation switch 2204, and a display 2205. The electro-optic device of the invention in this application can be used for a display 2205, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0265] Drawing 23 (D) is a goggles mold display, and consists of a body 2301, a display 2302, and the arm section 2303. The electro-optic device of the invention in this application can be used for a display 2302, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0266] Drawing 23 (E) is a rear projector (projection TV), and consists of a body 2401, the light source 2402, a liquid crystal display 2403, a polarization beam splitter 2404, reflectors 2405 and 2406, and a screen 2407. This invention can be used for a liquid crystal display 2403, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0267] Drawing 23 (F) is a front projector and consists of a body 2501, the light source 2502, a liquid crystal display 2503, optical system 2504, and a screen 2505. This invention can be used for a liquid crystal display 2503, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0268] Drawing 24 (A) is a personal computer and contains a body 2601, the image input section 2602, a display 2603, and keyboard 2604 grade. The electro-optic device of the invention in this application can be used for a display 2603, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0269] Drawing 24 (B) is an electronic play device (game device), and contains a body 2701, a record medium 2702, a display 2703, and a controller 2704. The voice outputted from this electronic game device and an image are reproduced on the display display containing a case 2705 and a display 2706. A wire communication, radio, or optical communication can be used for the means of communications between a controller 2704 and a body 2701, or the means of communications between an electronic game device and a display display. In this example, it has composition which detects infrared radiation in the sensor sections 2707 and 2708. The electro-optic device of the invention in this application can be used for displays 2703 and 2706, and the semiconductor circuit of the invention in this application can be used for CPU, memory, etc.
[0270] Drawing 24 (C) is a player (picture reproducer) using the record medium (it is hereafter called a record medium) which recorded the program, and includes a body 2801, a display 2802, the loudspeaker section 2803, a record medium 2804, and the actuation switch 2805. In addition, this picture reproducer can use music appreciation, movie appreciation, a game, and the Internet, using DVD (Digital VersatileDisc), CD, etc. as a record medium. The electro-optic device of the invention in this application can be used for a display 2802, CPU, memory, etc.
[0271] Drawing 24 (D) is a digital camera and contains a body 2901, a display 2902, an eye contacting part 2903, the actuation switch 2904, and the television section (not shown). The electro-optic device of the invention in this application can be used for a display 2902, CPU, memory, etc.
[0272] In addition, the detailed explanation about the optical engine which can be used for the rear projector of drawing 23 (E) or the front projector of drawing 23 (F) is shown in drawing 25 . In addition, drawing 25 (A) is an optical engine and drawing 25 (B) is light source optical system built in an optical engine.
[0273] The optical engine shown in drawing 25 (A) contains the light source optical system 3001, mirrors 3002, 3005-3007, dichroic mirrors 3003 and 3004, optical lenses 3008a-3008c, prism 3011, a

liquid crystal display 3010, and the incident light study system 3012. The incident light study system 3012 is the optical system equipped with the projector lens. Although this example showed the example of the 3 plate type which uses three liquid crystal displays 3010, it may be a veneer type. Moreover, a film or IR film for adjusting an optical lens, the film which has a polarization function, and phase contrast to the optical path shown by the arrow head etc. may be prepared into drawing 25 (A).
[0274] Moreover, as shown in drawing 25 (B), the light source optical system 3001 contains the light sources 3013 and 3014, the synthetic prism 3015, collimator lenses 3016 and 3020, the lens arrays 3017 and 3018, and the polarization sensing element 3019. In addition, although the light source optical system shown in drawing 25 (B) used the two light sources, the number of it one and it is good also as three or more. Moreover, an optical lens, the film which has a polarization function, the film which adjusts phase contrast, or IR film may be prepared in somewhere in optical paths of light source optical system.
[0275] As mentioned above, the applicability of the invention in this application is very wide, and applying to the electric appliance of all fields is possible. Moreover, even if the electric appliance of this example uses the configuration which consists of combination like an example 1 - 19 throats, it is realizable.
[0276] [Example 21] Drawing 26 is a graph (henceforth an ID-VG curve) showing the relation of the drain current (ID) of the n channel mold TFT302 and gate voltage (VG) which were produced according to the example 1, and the graph of electric field effect mobility (micro FE). At this time, the source electrical potential difference (VS) set 0V and a drain electrical potential difference (VD) to 1V or 14V. In addition, for channel length (L), 7.5 micrometers and channel width (W) was [the thickness (Tox) of the actual measurement of 7.8 micrometers and gate dielectric film] 110nm.
[0277] In drawing 26 , although, as for the thick wire, the dotted line showed the ID-VG curve and electric field effect mobility after a stress test before the stress test, it is almost changeless on a curve before and behind a stress test, and it turned out that hot carrier degradation is controlled. In addition, the stress test performed here is a trial held for 60 seconds where source electrical-potential-difference 0V, drain electrical-potential-difference 20V, and gate voltage 2V are applied at a room temperature, and is a trial which promotes hot carrier degradation.
[0278]
[Effect of the Invention] By using the invention in this application, it can become possible to arrange the circuit of the suitable engine performance on the same substrate according to the specification which a circuit requires, and the engine performance of operation and dependability of an electro-optic device can be raised sharply.
[0279] Moreover, in the pixel section of the electro-optic device represented by the liquid crystal display, the retention volume which has a big capacity in a small area can be formed. Therefore, it becomes possible to secure sufficient retention volume, without reducing a numerical aperture also in the electro-optic device of 1 inch or less of vertical angles.
[0280] Moreover, the engine performance of operation and dependability of an electric appliance which have such an electro-optic device as a display can also be raised.

[Translation done.]

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 2] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 3] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 4] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 5] Cross-section structural drawing of an active matrix liquid crystal display.
[Drawing 6] Drawing showing the LDD structure of the n channel mold TFT.
[Drawing 7] Drawing showing the LDD structure of the n channel mold TFT (pixel TFT).
[Drawing 8] The perspective view of an active matrix liquid crystal display.
[Drawing 9] The circuit block diagram of an active matrix liquid crystal indicating equipment.
[Drawing 10] Drawing showing the top-face structure of the pixel section.
[Drawing 11] Drawing showing the cross-section structure and top-face structure of the pixel section.
[Drawing 12] Drawing showing the structure of retention volume.
[Drawing 13] The sectional view showing the configuration of retention volume.
[Drawing 14] Drawing showing the LDD structure of the n channel mold TFT (pixel TFT).
[Drawing 15] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 16] Drawing showing the production process of the pixel section and a drive circuit.
[Drawing 17] Drawing showing the configuration of a active-matrix mold EL display.
[Drawing 18] Drawing showing the top-face structure and cross-section structure of EL display.
[Drawing 19] Drawing showing the cross-section structure of EL display.
[Drawing 20] Drawing showing the top-face structure of the pixel section of EL display.
[Drawing 21] Drawing showing the cross-section structure of EL display.
[Drawing 22] Drawing showing the circuitry of the pixel section of EL display.
[Drawing 23] Drawing showing an example of an electric appliance.
[Drawing 24] Drawing showing an example of an electric appliance.
[Drawing 25] Drawing showing the configuration of an optical engine.
[Drawing 26] Drawing showing the Id-Vg curve of TFT.

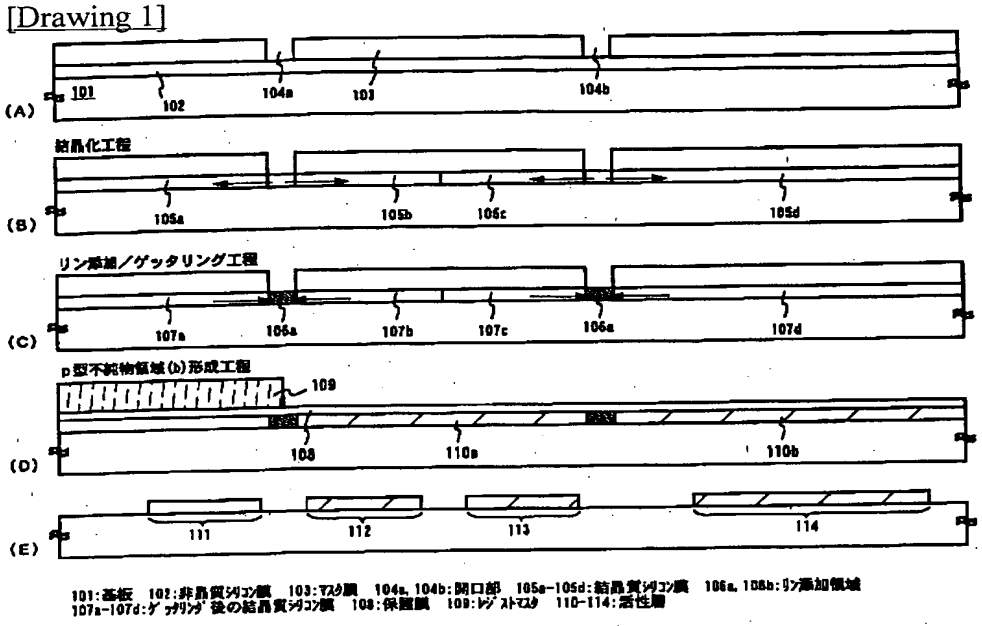
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

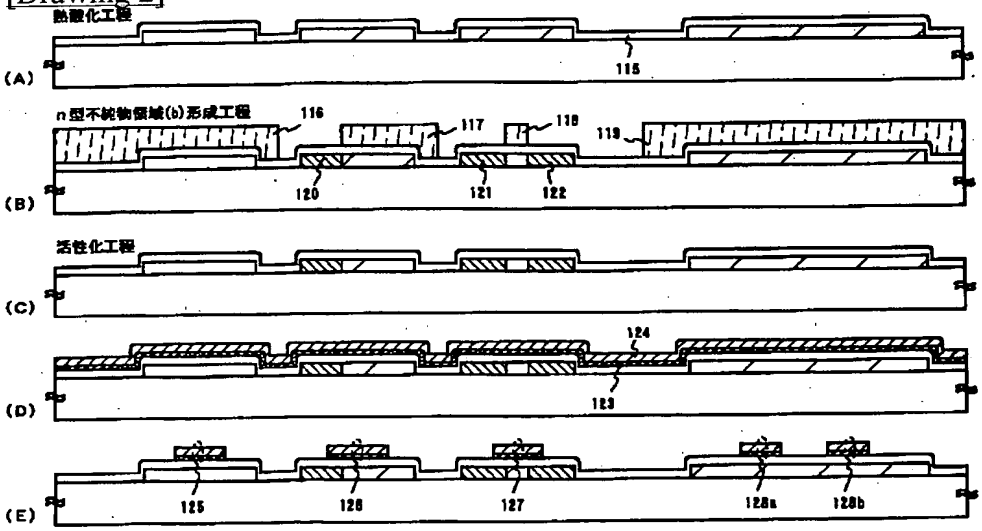
DRAWINGS

[Drawing 1]



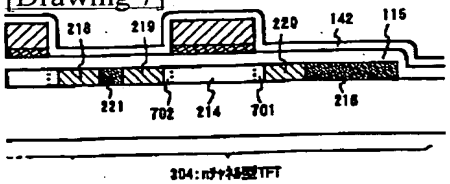
101:基板 102:非晶質シリコン膜 103:マスク膜 104a, 104b:開口部 105a-105d:結晶質シリコン膜 106a, 106b:リン添加領域
107a-107d:ゲッタリング後の結晶質シリコン膜 108:保護膜 109:レジストマスク 110-114:活性層

[Drawing 2]

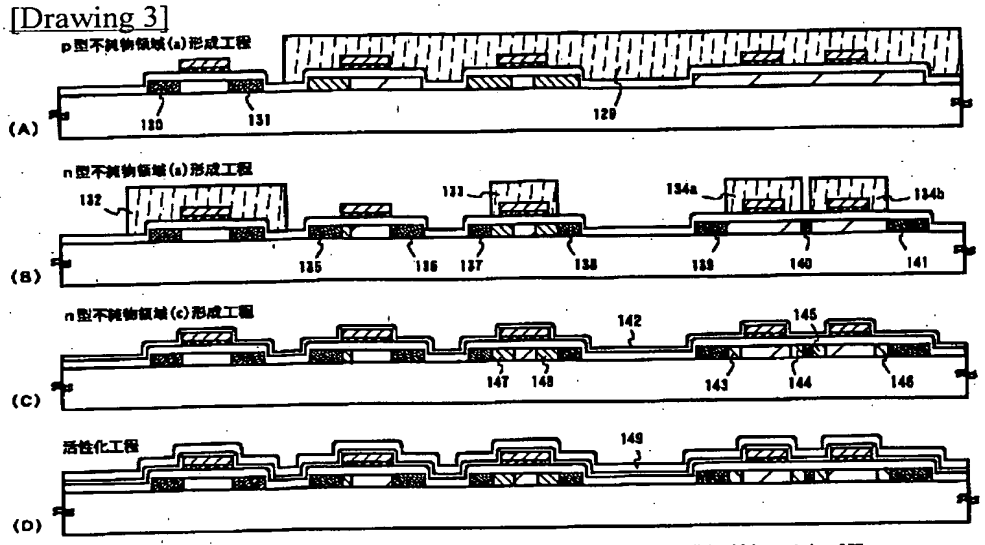


115:ゲート絶縁膜 116-119:レジストマスク 120-122: n型不純物領域(b) 123:第1導電膜
124:第2導電膜 125-128:ゲート配線

[Drawing 7]

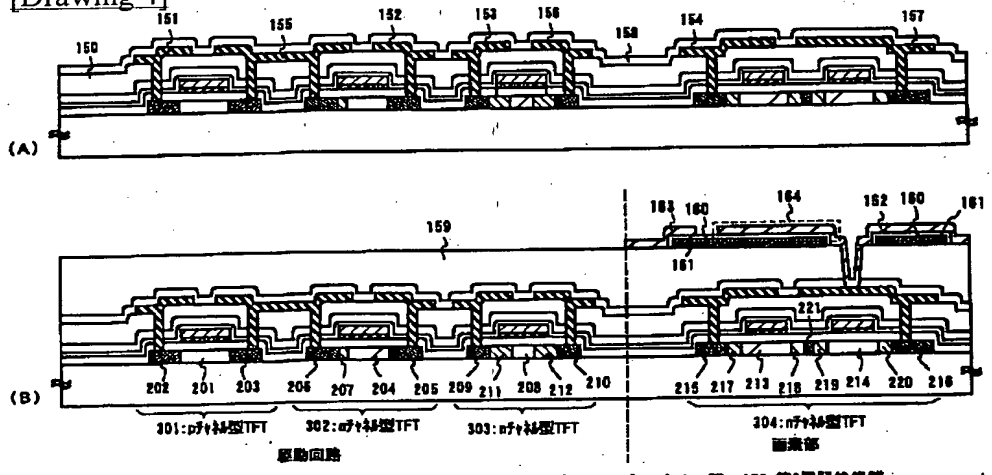


[Drawing 3]



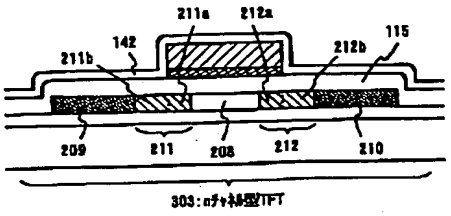
129, 132-134:レジストマスク 130, 131: p型不純物領域(a) 135-141: n型不純物領域(a) 142:キャップ膜
143-146: n型不純物領域(c) 147, 148: n型不純物領域(b) 149:第1層間絶縁膜

[Drawing 4]

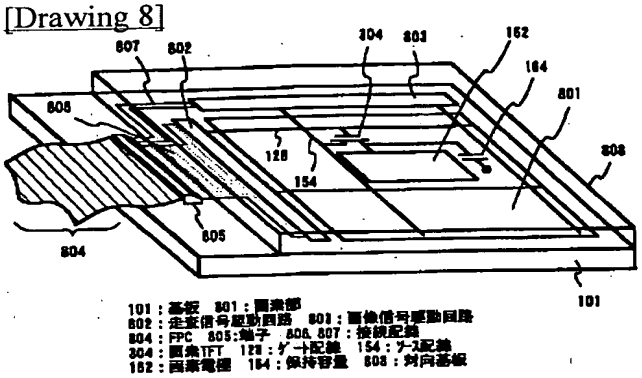


150:第2層間絶縁膜 151-154:ソース配線 155-157:ドレイン配線 158:パッシベーション膜 159:第3層間絶縁膜
160:透明導電膜 161:陽極酸化物 162, 163:画素電極 164:保持容量
201, 204, 208, 213, 214:チャネル形成領域 202, 205, 209, 215:ソース領域 203, 206, 210, 218:ドレイン領域
207, 211, 212: n型不純物領域(b) 217-220: n型不純物領域(c) 221: n型不純物領域(a)

[Drawing 6]



[Drawing 8]



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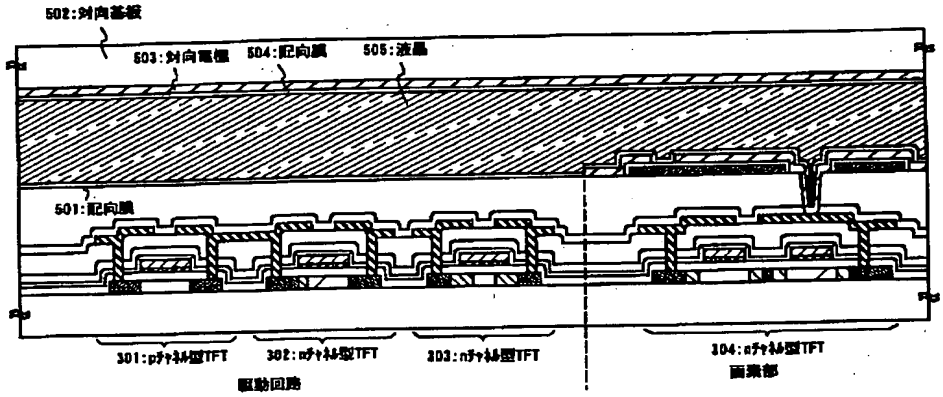

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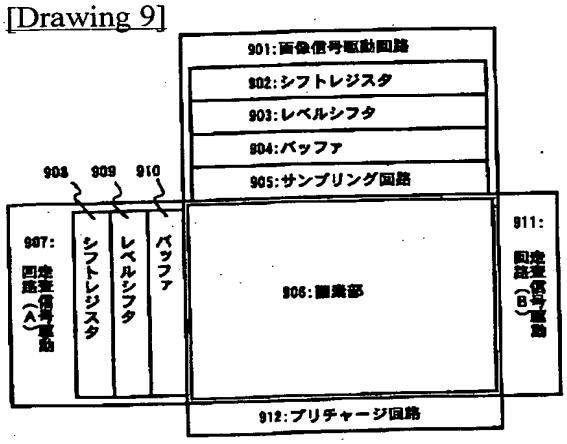

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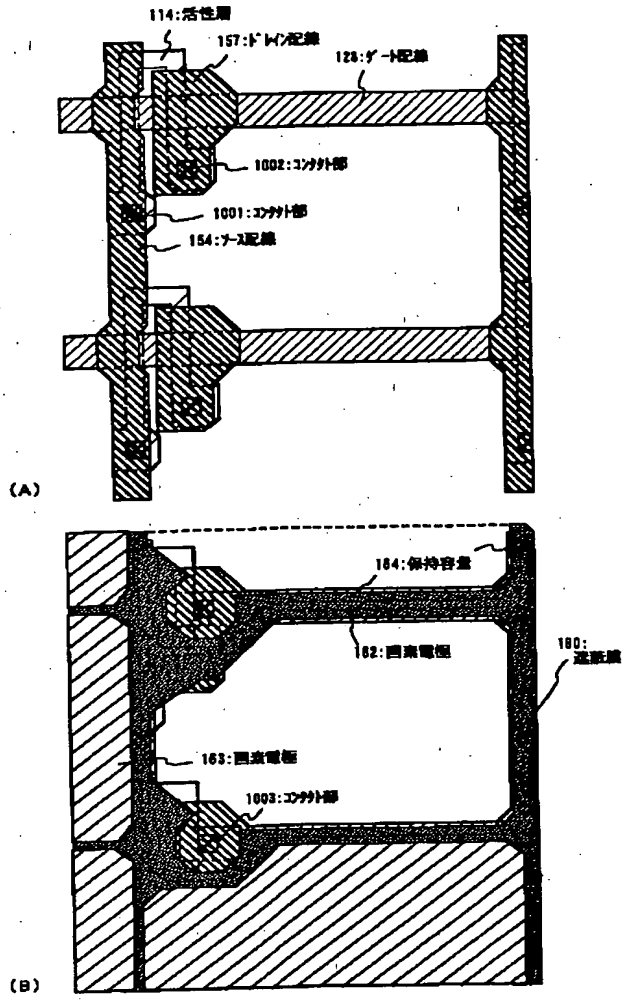

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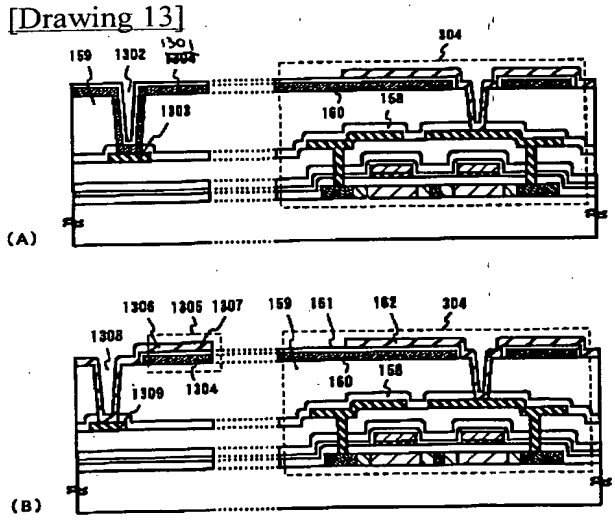
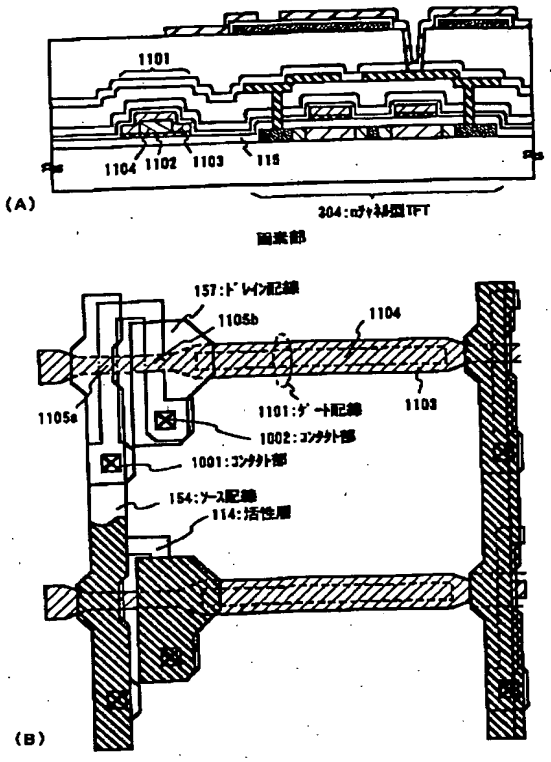
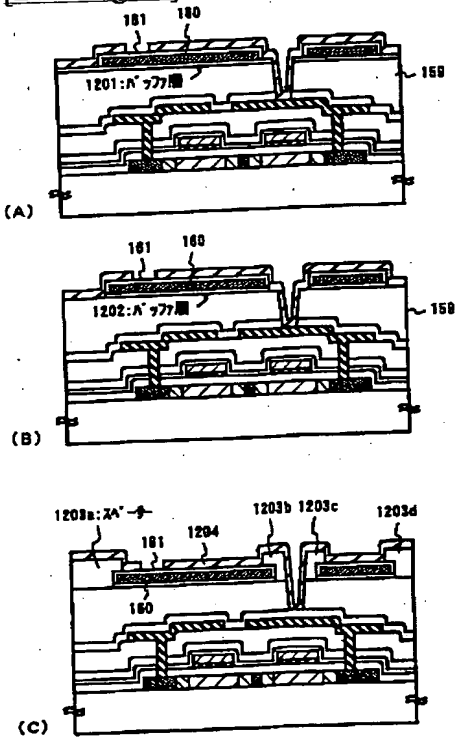


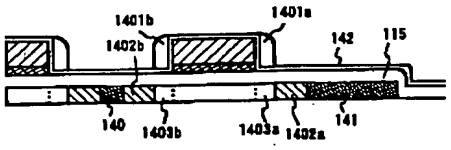
[Drawing 11]



[Drawing 12]

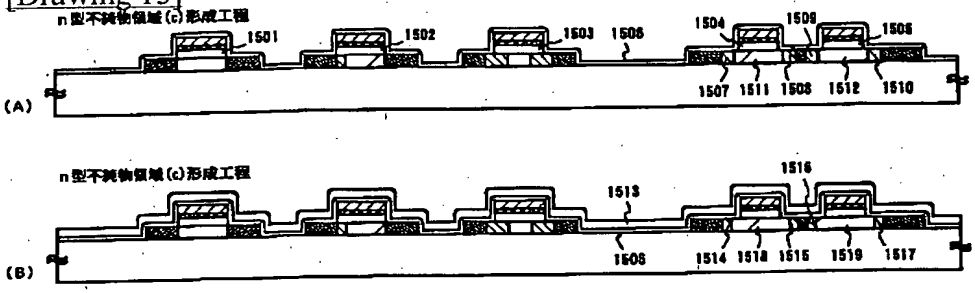


[Drawing 14]

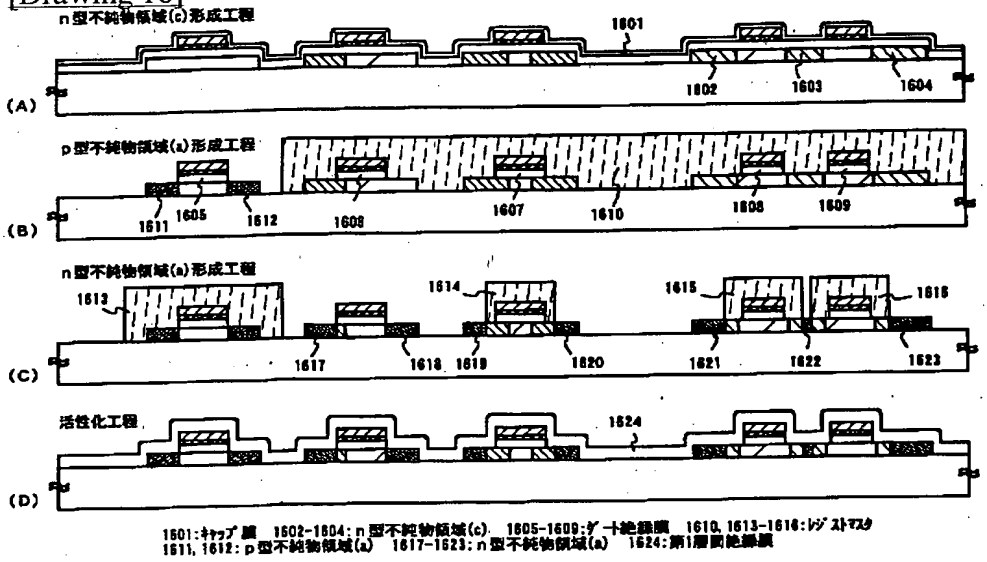


115:ゲート絶縁膜　140, 141: n型不純物領域(a)　142:キャップ膜
1401a, 1401b:サイドウォール　1402a, 1402b: n型不純物領域(c)
1403a, 1403b:オフセット領域

[Drawing 15]

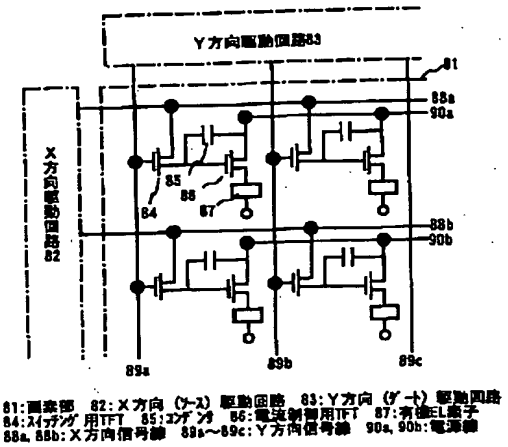


[Drawing 16]



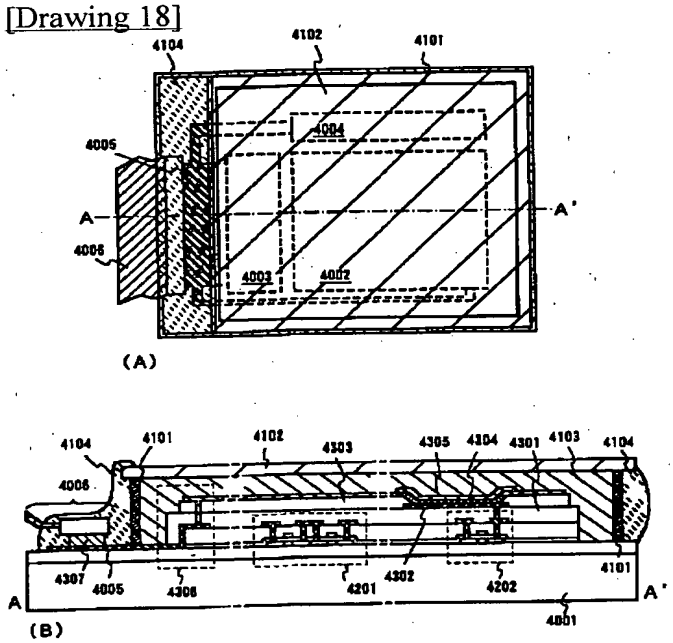
1601:キャップ膜　1602-1604: n型不純物領域(c)　1605-1609:ゲート絶縁膜　1610, 1613-1616:レジストマスク
1611, 1612: p型不純物領域(a)　1617-1623: n型不純物領域(a)　1624:第1層間絶縁膜

[Drawing 17]

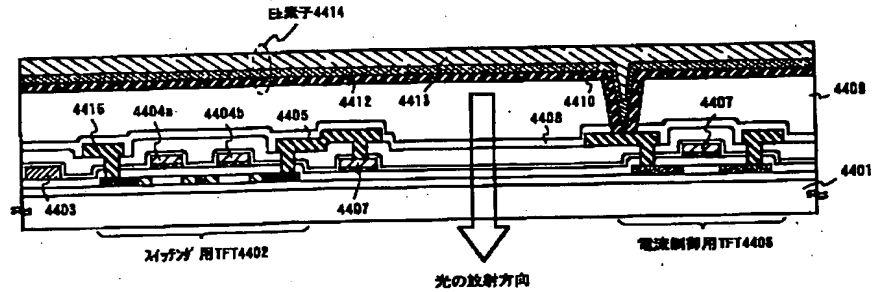


81:画素部 82:X方向（ソース）駆動回路 83:Y方向（ゲート）駆動回路
84:スイッチング用TFT 85:コンデンサ 86:電流制御用TFT 87:有機EL素子
88a, 88b:X方向信号線 89a～89c:Y方向信号線 90a, 90b:電源線

[Drawing 18]



[Drawing 19]



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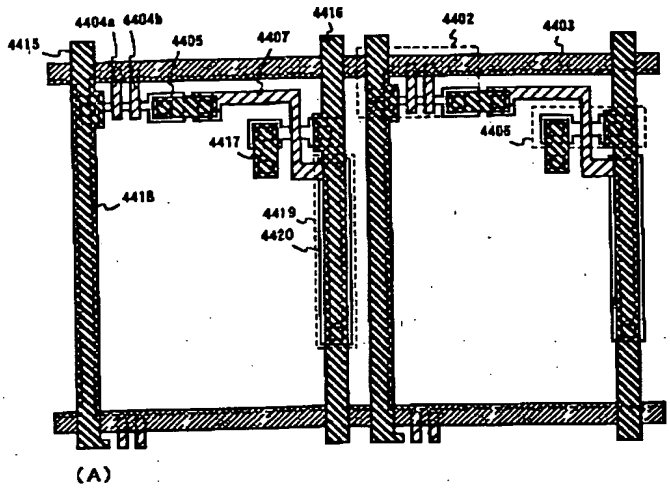
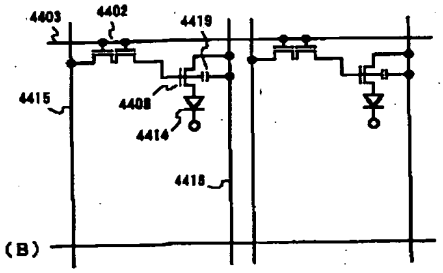
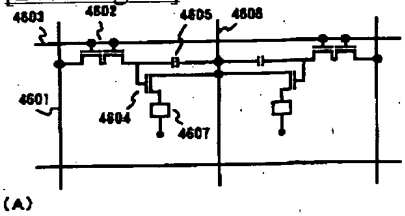
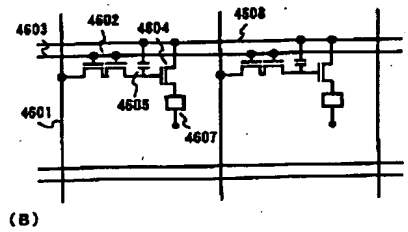
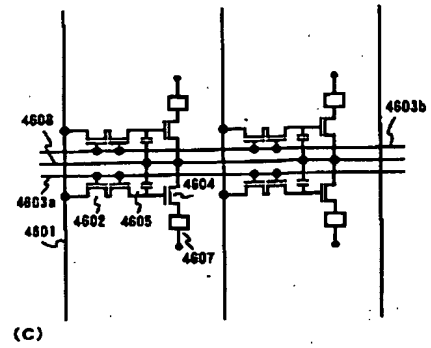

4404a
4404b
4416
4402
4403
4415
4405
4407
4417
4405
4418
4419
4420
(A)


4403
4402
4419
4415
4408
4414
4418
(B)

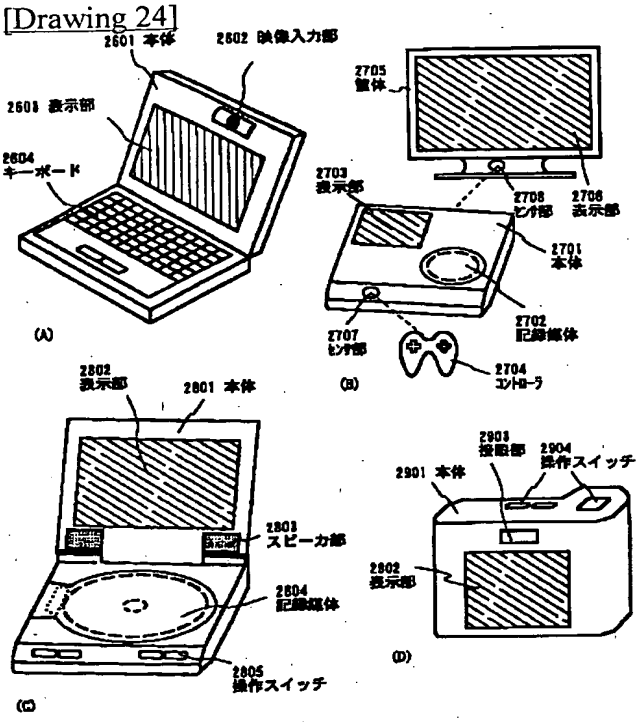
[Drawing 22]


4603
4602
4605
4606
4601
4604
4607
(A)

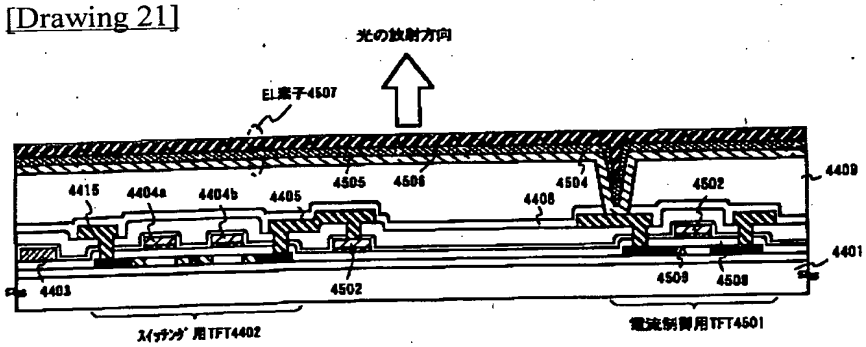

4603
4602
4604
4606
4605
4601
4607
(B)


4606
4603b
4604
4603a
4602
4605
4601
4607
(C)

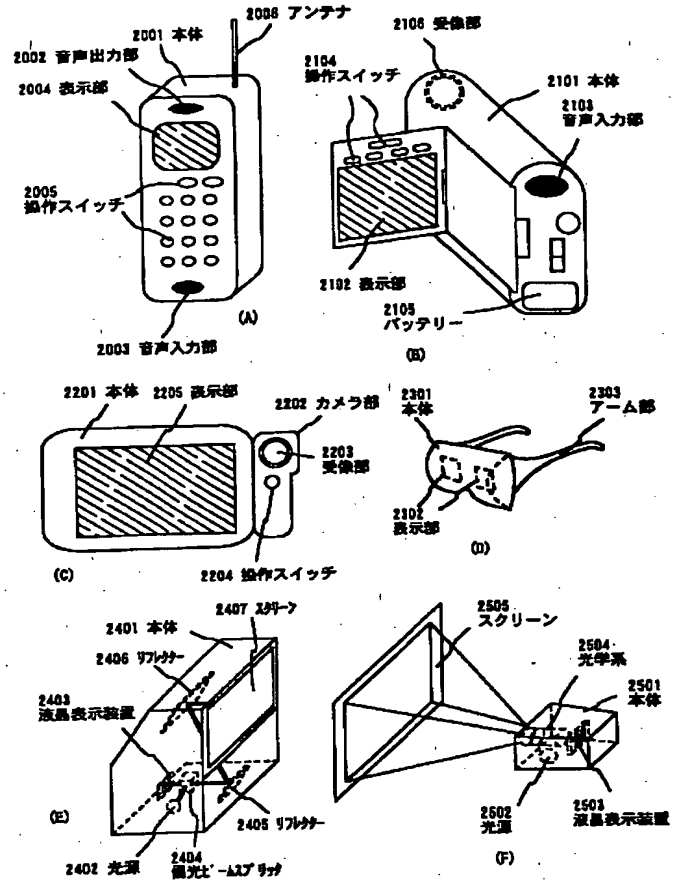
[Drawing 24]



[Drawing 21]



[Drawing 23]



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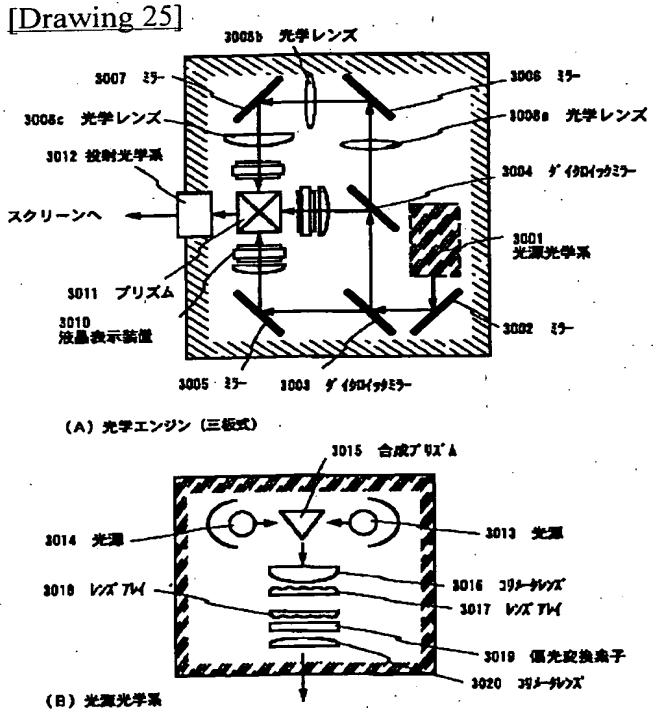
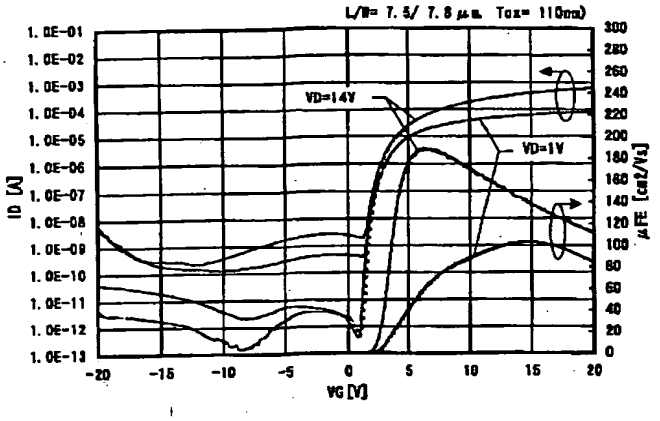


[Drawing 26]



[Translation done.]